IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants.	Civil Action No. 06-726 (JJF) Civil Action No. 07-357 (JJF) CONSOLIDATED CASES

DEFENDANT CHI MEI OPTOELECTRONICS CORPORATION'S REPLY BRIEF IN SUPPORT OF ITS MOTION TO LIMIT THE NUMBER OF PATENTS-IN-SUIT AND STAY THE REMAINDER

OF COUNSEL:

Jonathan S. Kagan
Alexander C.D. Giza
Adam Hoffman
Irell & Manella LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067-4276
(310) 277-1010

Philip A. Rovner (#3215)
POTTER ANDERSON & CORROON LLP
Hercules Plaza
1313 N. Market St.
P.O. Box 951
Wilmington, Delaware 19899-0951
(302) 984-6000
provner@potteranderson.com

Attorneys for Defendant
Chi Mei Optoelectronics Corporation

Dated: September 2, 2008

TABLE OF CONTENTS

Page

I. INTRODUCTION 1

II. AN IMMEDIATE STAY WILL CONSERVE JUDICIAL RESOURCES AND BENEFIT THE PARTIES 3

III. LGD'S PROPOSAL, NOT CMO'S, WOULD RESULT IN UNDUE PREJUDICE AND A TACTICAL DISADVANTAGE 6

A. CMO's Proposal Would Not Cause LGD Undue Prejudice 6

B. By LGD's Own Standards, The Court Should Limit The Parties To An Equal Or Proportional Number Of Patents 8

(1) LGD Miscounts Its Number Of Asserted Patents 9

(2) LGD's Proposal Is Unfair And Unbalanced 9

IV. CONCLUSION 11

TABLE OF AUTHORITIES

Page(s)

Cases

ASM Am., Inc. v. Genus, Inc.,
2002 WL 24444 (N.D. Cal. Jan. 9, 2002) 6

Enzo Life Sci., Inc. v. Digene Corp.,
2003 WL 21402512 (D. Del. June 10, 2003) 8

Honeywell Int'l Inc. v. Audiovox Commc'n Corp.,
2005 WL 2465898 (D. Del. May 18, 2005) 4, 8

Hunter Eng'g Co. v. ACCU Indus., Inc.,
245 F. Supp. 2d 761 (E.D. Va. 2002) 7

Johns Hopkins Univ. v. Cellpro,
160 F.R.D. 30 (D. Del. 1995) 7

Network Appliance Inc. v. Sun Microsystems Inc.,
2008 WL 2168917 (N.D. Cal. May 23, 2008) 7

Rules

Rule 42(b) 8

I. INTRODUCTION

None of the parties to this case dispute the central problem that underlies CMO's motion—that this case involves too many patents from too many parties for it to proceed as an ordinary patent case. The numbers speak for themselves: the case involves twenty-three patents asserted by three separate parties. As reflected in the parties' joint claim construction chart, hundreds of claim elements are at issue, and the parties have addressed approximately 200 of those disputed elements in their opening *Markman* briefing.

By any measure, be it the number of patents and claims asserted, the diverse nature of the technology (covering semiconductor fabrication, circuit layouts, optics, and assembly lines), or the number of accused products, this is a complicated case, and, quite possibly, one of the largest patent case ever before the Court. Absent a partial stay, going forward toward trial in June 2009, the attention of the parties and the Court will be diverted among the multitude of asserted technologies, complicating discovery, claim construction, expert reports, and summary judgment. Separate trials will almost certainly be necessary, if only to simplify issues for the jury. Given this inescapable reality, a partial stay of asserted patents at this point will help conserve the resources of the parties and the Court.

CMO's proposal of initially limiting the parties to four patents each and three claims per patent, staying the remainder for later trial, eliminates any tactical advantage one party might try to gain over the others in the initial trial, while allowing all parties to preserve each of their infringement claims. In their opposition briefs, LGD and AUO agree that staying some asserted patents may be appropriate. However, AUO seeks to inefficiently delay a stay, while LGD agrees with a stay but suggests an overwhelmingly lopsided patent allocation at the initial trial, which is clearly designed to try to provide LGD with an unfair strategic advantage, rather than eliminating any potential prejudice, per CMO's proposal.

AUO suggests that patents should be stayed only after the parties and the Court have invested months of additional effort into claim construction, discovery, and expert reports. *See* AUO's Answering Brief ("AUO Opp.") at 6 ("[P]atents should be stayed (if at all) after claim construction and after discovery is complete."); *id.* at 1 ("AUO agrees that there will likely be a time when the parties should narrow this case . . . ."). This inefficient proposal turns the standard for a stay, under which a stay is least appropriate after discovery is complete, on its head.

LGD opposes staying patents unless the number of patents is reduced by four per party. Under LGD's calculations, LGD would be permitted to assert five patents against CMO at the initial trial, while CMO would assert only two of its patents. CMO does not believe this would make for a balanced presentation at trial, and it would instead provide LGD with a tactical advantage, defensively and offensively. The formula LGD used to craft its proposal shows that LGD is well aware that it is seeking a disproportionate advantage at trial: LGD proposes that the Court reduce the number of patents LGD is being accused of infringing by eight, double the four-patent reduction for each of the other parties. LGD's aggressive math seems aimed particularly at CMO: under LGD's plan, CMO's asserted patents would be reduced by *four*, from six to two, a two-thirds reduction, while LGD's patents asserted against CMO would only be reduced by only *three*, from eight to five, a reduction of less than half.[1] LGD further proposes that the parties be limited to an average of three claims per patent across all non-stayed patents, allowing LGD to assert fifteen claims culled from its strongest patents against CMO, while CMO

[1] CMO's infringement claims were only asserted in the action transferred from Texas (the "Texas action"), which remains a separate action with a separate scheduling order. CMO's patents are currently at issue in this case in a limited way, by virtue of LGD's claims for declarations of invalidity. However, the parties agree that the Texas action should be consolidated with this one, and for the purposes of this motion, CMO assumes, as does LGD, that the infringement claims will soon be added to this case.

would only assert a total of six claims period. LGD's proposal would create prejudice at the initial trial, rather than place the parties on even footing.

II. AN IMMEDIATE STAY WILL CONSERVE JUDICIAL RESOURCES AND BENEFIT THE PARTIES

LGD and AUO attack a straw-man, deliberately misconstruing CMO's argument to mean that the Court must now construe hundreds of disputed claim elements. For example, citing to a footnote in CMO's Opening Brief, LGD states that it "disagrees with CMO's suggestion that the Court is required to construe three hundred disputed claim terms in this case." LGD Opp. at 5 (citing CMO's Opening Brief at 5 n.1); *see also* AUO Opp. at 6 ("CMO's reading of the law is completely incorrect. The Court does not need to construe anywhere near 300 claim elements.").

As reflected in the very footnote LGD cites, however, CMO does not argue that the Court must construe 300 claim elements. *See* CMO's Opening Brief at 5 n.1 ("CMO does not contend that *Markman* and *O2 Micro* require the Court to construe *every* claim element . . . .") (emphasis in original). In light of the Court's obligation to resolve a fundamental dispute regarding the scope of a claim element—an obligation neither LGD nor AUO disputes—it is simply more efficient to limit the parties to an equal number of asserted patents and claims now, as opposed to construing hundreds of disputed elements in advance or revisiting claim construction when a fundamental dispute bearing on infringement or validity is presented later in the case. *See, e.g., id.* at 5. It is likewise more efficient to focus the Court and the parties on a more limited subset of patents and claims, as CMO proposes, rather than moving forward with claim construction, depositions, and expert reports on an unlimited number of claim elements from twenty-three separate patents.

While LGD and AUO both acknowledge the inefficiencies in attempting to proceed on all patents and claims simultaneously at trial, neither presents a practical solution that will

address these problems. AUO's proposal that "patents should be stayed (if at all) after claim construction and after discovery is complete," AUO Opp. at 6, would impose too substantial a burden on the parties and the Court. Contrary to AUO's suggestion, a stay is most appropriate earlier in litigation, before the parties and the Court invest further effort into patents and claims that will be stayed. *See Honeywell Int'l Inc. v. Audiovox Commc'n Corp.*, No. Civ. A. 04-1337-KAJ et al., 2005 WL 2465898, at *2 (D. Del. May 18, 2005 (noting that courts consider "whether discovery is completed" in evaluating motions for a stay).

AUO offers three case-management alternatives to an immediate partial stay, each of which fails to ameliorate the inefficiencies of a later stay. AUO suggests that the Court (1) "construe terms addressed in the parties' briefing and set aside other terms until [sic] if and when a real dispute arises;" (2) "requir[e] the parties to identify a limited number of terms for construction that are 'fundamental' to the dispute;" or (3) "require the parties to explain, for each claim offered for construction, why construction of the term is potentially outcome determinative." AUO Opp. at 7. The first proposal would require the Court to construe all the claim elements in the parties' *Markman* briefing, while leaving open the possibility that the Court would nevertheless revisit claim construction "when a real dispute arises," possibly in the midst of expert reports or even trial. The second and third proposals are grossly inefficient, forcing the parties and the Court to continue to divert their efforts among twenty-three patents.

Even the factual assumptions behind AUO's position are unsound. AUO suggests that the *Markman* briefing page limits have "already effectively forced the parties to focus only upon terms that matter." *Id.* at 7. In fact, the *Markman* briefing demonstrates how unfocused this case will be without a partial stay: the parties have packed approximately 200 elements into their opening *Markman* briefing, and as evidenced by the joint claim construction chart, this is only a

subset of the hundreds of elements the parties consider material. While AUO argues that the main detriment to a partial stay is that it will delay settlement, *id.* at 4, in fact, a partial stay will advance settlement by focusing the parties on the patents and claims they deem most critical. Even if the parties fail to reach a full global settlement before trial next June, the remaining patents will have been stayed a mere nine months, not indefinitely, as AUO contends.

LGD's proposal fares even worse. LGD suggests that the Court sift through hundreds of pages of *Markman* briefing so that the Court, acting independently, can identify dispositive claim elements spread over twenty-three patents, without the benefit of infringement or invalidity contentions. *See* LGD Opp. at 6 (noting that "this Court has previously chosen to construe only those disputed elements that are dispositive to the issues in the case" and recommending that the Court do so here). This is not a realistic burden to impose on this Court, particularly because LGD's proposal would still leave all twenty-three patents and an unlimited number of claim elements in play.

Even LGD does not propose this as a serious alternative. Rather, LGD devotes most of its brief to an alternative proposal, noting that it is "amenable" to a reduction in the number of patents and claims if the outcome is "fair and balanced," LGD Opp. at 6, which to LGD means that it should be afforded a roughly equal number of patents (five) to that of the two other parties combined (two for CMO and four for AUO). LGD goes so far as to state that even after its proposed twelve-patent stay, a further stay of asserted patents may be necessary. *Id.* at 10 n.8. The obvious impact of LGD's self-proclaimed "fair and balanced" proposal is that LGD would appear at the initial trial to have far more patents than either CMO or AUO. Whether or not this would make a difference to a jury, the Court can eliminate any possible claim of prejudice by

allowing each party the same number of patents and claims at the initial trial, as CMO has proposed.

III. LGD'S PROPOSAL, NOT CMO'S, WOULD RESULT IN UNDUE PREJUDICE AND A TACTICAL DISADVANTAGE

LGD contends that it would suffer undue prejudice and be at a tactical disadvantage if the parties are limited to an equal number of patents and claims. LGD instead proposes that if there is a reduction in the number of asserted patents, the Court should reduce CMO's patents by *four*, from six to two, a two-thirds reduction, while reducing LGD's patents currently asserted against CMO by *three*, from eight to five, a reduction of less than half. As explained below, LGD's contention fails, and its prejudicial proposal should be rejected.

A. CMO's Proposal Would Not Cause LGD Undue Prejudice

LGD fails to identify any cognizable prejudice that would result from limiting the parties to an *equal number* of asserted patents and claims. In fact, LGD stands to benefit from CMO's proposal. Under CMO's proposal of four patents for each party, LGD would have to defend against *six* fewer patents—four of AUO's eight patents would be stayed and two of CMO's patents would be stayed—while asserting only *four* fewer patents against CMO. AUO, for its part, would face a similar reduction in asserted patents as LGD, without the same defensive benefits.

Nevertheless, LGD contends that limiting the parties to an equal number of asserted patents would prejudice it by causing more of its patents to be stayed than CMO. LGD's contention fails. While CMO's proposed stay will affect all parties' claims and be lifted nine months from now, after trial next June, courts grant bifurcations and stays even where the bifurcation and stay would only affect one party's claims and add years to the litigation. *See, e.g., ASM Am., Inc. v. Genus, Inc.*, No. 01-2190 EDL, 2002 WL 24444, at *6 (N.D. Cal. Jan. 9,

2002) (noting that "[i]t is a common practice in federal court to stay antitrust counterclaims until after the trial of the invalidity issue" and collecting cases); *Johns Hopkins Univ. v. Cellpro*, 160 F.R.D. 30, 34 (D. Del. 1995) (noting that "cases suggest that the courts (and perhaps the parties) found the benefit of deferring the time and expense of work on damages in patent cases until after liability had been determined outweighed the cost of a delay in the resolution of the case, even if that delay deferred a final resolution in favor of the patent owner for eight, ten or twelve years").

The only authority LGD cites to support the notion that it will suffer prejudice, *Network Appliance Inc. v. Sun Microsystems Inc.*, No. C-07-06053-EDL, 2008 WL 2168917 (N.D. Cal. May 23, 2008), undercuts LGD's argument. The Court in *Network Appliance* stayed patent claims from only one party, on fact less compelling than here, where CMO's proposed stay would affect all parties. In *Network Appliance,* a defendant moved to stay three of the plaintiff's seven patents pending their reexamination while continuing to move forward on all twelve of its own asserted patents. The court noted that the plaintiff "will face a tactical disadvantage if [the defendant] is permitted to *make its tactical decision as to which claims to pursue most aggressively in this litigation from all of the patents that it has asserted*, while [the plaintiff] is forced to litigate only four of its seven asserted patents." *Id.* at *5 (emphasis added). The court nevertheless stayed one patent because the PTO had already issued an office action rejecting the patent's claims, allowing the defendant to renew its motion "if there is a significant change in the reexamination status" of the other patents. *Id.* at *5-6. Here, in contrast, all parties will face the same tactical decision of determining which patents and claims to pursue; no party would face a tactical advantage over the others. *Cf. Hunter Eng'g Co. v. ACCU Indus., Inc.*, 245 F. Supp. 2d 761, 764 n.1 (E.D. Va. 2002) (noting that after the parties briefed eighteen patents-in-suit for

claim construction, "Judge Adelman asked each side to submit two of their own patents and one of their opponent's patents," staying the remaining twelve patents).

While CMO's proposal does not prejudice LGD, undue prejudice, the only factor that LGD argues in its brief, is one of several factors typically considered in connection with a request for a stay. LGD's slight alleged prejudice does not trump other considerations that warrant a bifurcation and stay here, such as the simplification of issues and the conservation of judicial resources. *See Honeywell Int'l Inc. v. Audiovox Commc'n Corp.*, No. Civ. A. 04-1337-KAJ et al., 2005 WL 2465898, at *2 (D. Del. May 18, 2005) ("When considering a motion to stay, the court considers the following factors: (1) whether a stay would unduly prejudice or present a clear tactical disadvantage to the non-moving party; (2) whether a stay will simplify the issues and trial of the case; (3) whether discovery is completed; and (4) whether a trial date has been set."); *Enzo Life Sci., Inc. v. Digene Corp.*, No. Civ. A. 02-212-JJF, 2003 WL 21402512, at *4 (D. Del. June 10, 2003) (Farnan, J.) ("Courts, when exercising their broad discretion to bifurcate issues for trial under Rule 42(b), should consider whether bifurcation will avoid prejudice, conserve judicial resources, and enhance juror comprehension of the issues presented in the case.").

B. By LGD's Own Standards, The Court Should Limit The Parties To An Equal Or Proportional Number Of Patents

LGD claims that the proper approach "should impact all parties equally;" achieve "a fair and balanced reduction of patents and claims" that is "neutral and leave[s] the parties in the same posture as currently exists;" and "account for and preserve the relative positions of the parties now." LGD Opp. at 3, 8, 9. LGD suggests that a stay would meet these standards if each party's asserted patents is reduced by four, which by LGD's calculations means that it would assert five patents against AUO and CMO (from nine currently asserted against AUO and eight against

CMO), while AUO is limited to four patents (from eight patents) and CMO is limited to two patents (from six patents). Judged by its own standards, LGD's proposal fails.

(1) LGD Miscounts Its Number Of Asserted Patents

LGD's calculations begin with a sleight of hand. LGD counts United States Patent No. 6,664,569 against CMO among its currently asserted patents, despite its pending opposed motion to amend its pleadings to assert that patent against CMO, D.I. 303. If all patents are reduced equally, by its own standards, LGD would assert four, not five, patents against CMO.

Furthermore, among its nine patents currently asserted, LGD includes three from the same family, United States Patent Nos. 7,176,489, 6,815,321, and 5,905,274 (the "'274 patent"). These patents share substantially identical specifications. *See* Exs. A, B, C (attaching patents). Moreover, CMO and AUO treated the '274 patent family's disputed elements together in their claim construction briefing, while LGD simply incorporated constructions for the '274 patent for the two other patents, with the exception of arguing that particular elements in the other patents were clerical errors. *See* D.I. 383 at 28-32 (CMO's brief); D.I. 378 at 43-49 (AUO's brief); D.I. 384 at 20-26 (LGD's brief). The parties will likely continue to treat the patents together in later analyses. It would therefore be unfair to treat all three, substantially similar patents from the '274 patent family the same as the other patents-in-suit. If the Court were to implement a fair four-patent reduction that preserves the parties' current positions, LGD would have at least one fewer patent to assert against CMO, and the patents from the '274 family would not be afforded the same weight as LGD's, CMO's, and AUO's other asserted patents.

(2) LGD's Proposal Is Unfair And Unbalanced

Putting aside LGD's arithmetic difficulties, LGD's proposal would impact the parties unequally, achieve an unfair and unbalanced reduction that favors LGD, and disregard and destroy the relative positions of the parties. LGD's proposal would drastically improve its

defensive case while relegating CMO's patents to an afterthought in the initial trial. Under LGD's proposal, LGD would benefit by staying four patents from two opponents, or eight of the fourteen patents asserted against it. CMO and AUO would each need to defend against *four* less patents, leaving LGD in a relative defensive position twice as advantageous as that of the other parties. Worse still, as reflected in the chart below, four out of CMO's six patents would be stayed, a two-thirds reduction, while only three of LGD's eight patents asserted against CMO would be stayed, a reduction of less than half, disregarding the parties' relative positions.

	LGD Patents	**CMO Patents**	**AUO Patents**
Number of Patents Currently Asserted	9 against AUO; 8 against CMO	6	8
Number of Patents Asserted Under LGD's Proposal	5 against each defendant	2	4
Percentage Reduction	44% against AUO; 37.5% against CMO	66%	50%

Beyond the number of patents asserted, LGD's proposal allows it to assert nearly three times as many claims as CMO. LGD proposes that each party assert an average of three claims per patent, allocated among the patents as they see fit. CMO would be reduced to only six claims, while LGD would have a total of fifteen claims, which it would be free to concentrate among its strongest patents. LGD could, for example, assert only one claim from each of its three weakest non-stayed patents, while asserting six claims each—the same as CMO's total under LGD's proposal—from its two strongest patents.[2] To put it another way, from each of its two strongest patents, LGD could assert as many claims as CMO has period, while maintaining three other patents-in-suit. LGD's proposal would therefore relegate CMO's patents to a footnote

[2] CMO does not, however, oppose allowing the parties to select an average of three claims per patent, as long as the parties are limited to an equal number of non-stayed patents. As it stands, allowing LGD to cherry-pick its best claims from its strongest patents while staying two-thirds of CMO's patents only compounds CMO's prejudice.

in the initial litigation. This result is particularly unjust because it was LGD that moved to transfer CMO's infringement case from Texas, where less patents were at issue, and having won that motion, it is now LGD that wishes to make CMO's infringement case an afterthought.

Thus, even under LGD's faulty assumption that the parties must face a reduction in the number of asserted patents that preserves their relative positions, LGD's proposal fails. Following LGD's logic, the Court could order all parties to reduce the amount of patents they asserted by one-third. Rounding to the nearest number and counting all the patents in the '274 patent family, CMO would proceed with four patents, LGD with five patents against CMO and six patents against AUO, and AUO with five patents. With a two-thirds reduction, CMO would elect two patents and LGD and AUO each would elect three patents. As it stands, LGD's proposal, which is grounded in faulty (or biased) arithmetic, would more than halve the number of patents against which it must defend while staying most of CMO's infringement case.

IV. CONCLUSION

For the forgoing reasons, CMO respectfully urges the Court to exercise its discretion to focus claim construction, discovery, and eventual trial on roughly half of the patents-in-suit—four patents for each party and three claims for each such patent—while staying all proceedings on the remaining patents-in-suit. If the Court in its discretion chooses to reduce the parties' patents equally, CMO respectfully urges the Court do so by limiting the number of patents proportionally for each side.

POTTER ANDERSON & CORROON LLP

OF COUNSEL:

Jonathan S. Kagan
Alexander C.D. Giza
Adam Hoffman
Irell & Manella LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067-4276
(310) 277-1010

Dated: September 2, 2008
880805

By: /s/ Philip A. Rovner
Philip A. Rovner (#3215)
Hercules Plaza
1313 N. Market St.
P.O. Box 951
Wilmington, Delaware 19899-0951
(302) 984-6000
provner@potteranderson.com

Attorneys for Defendant
Chi Mei Optoelectronics Corporation

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

CERTIFICATE OF SERVICE

I, Philip A. Rovner, hereby certify that on September 2, 2008, the within document was filed with the Clerk of the Court using CM/ECF which will send notification of such filing(s) to the following; that the document was served on the following counsel as indicated; and that the document is available for viewing and downloading from CM/ECF.

BY CM/ECF, HAND DELIVERY AND E-MAIL

Richard E. Kirk, Esq.
Ashley Blake Stitzer, Esq.
The Bayard Firm
222 Delaware Avenue
Suite 900
P.O. Box 25130
Wilmington, DE 19899
rkirk@bayardfirm.com
astitzer@bayardfirm.com

BY CM/ECF, HAND DELIVERY AND E-MAIL

John W. Shaw, Esq.
Karen L. Pascale, Esq.
Young Conaway Stargatt & Taylor LLP
The Brandywine Building
1000 West Street, 17th Floor
Wilmington, DE 19801
jshaw@ycst.com
kpascale@ycst.com

I hereby certify that on September 2, 2008 I have sent by E-mail the foregoing document to the following non-registered participants:

Gaspare J. Bono, Esq.
Matthew T. Bailey, Esq.
Lora A. Brzezynski, Esq.
Cass W. Christenson, Esq.
R. Tyler Goodwyn, IV, Esq.
McKenna Long & Aldridge LLP
1900 K Street, NW
Washington, DC 20006
gbono@mckennalong.com
mbailey@mckennalong.com
lbrzezynski@mckennalong.com
cchristenson@mckennalong.com
tgoodwyn@mckennalong.com

Vincent K. Yip, Esq.
Peter J. Wied, Esq.
Jay C. Chiu, Esq.
Katherine F. Murray, Esq.
Ms. Denise Esparza
Paul Hastings Janofsky & Walker LLP
515 South Flower Street
Los Angeles, CA 90071
vincentyip@paulhastings.com
peterwied@paulhastings.com
jaychiu@paulhastings.com
katherinemurray@paulhastings.com
deniseesparza@paulhastings.com

Ron E. Shulman, Esq.
Julie M. Holloway, Esq.
Wilson Sonsini Goodrich & Rosati
650 Page Mill Road
Palo Alto, CA 94304-1050
rshulman@wsgr.com
jholloway@wsgr.com

M. Craig Tyler, Esq.
Brian D. Range, Esq.
Wilson Sonsini Goodrich & Rosati
8911 Capital of Texas Highway North
Westech 360, Suite 3350
Austin, TX 78759
ctyler@wsgr.com
brange@wsgr.com

/s/ Philip A. Rovner
Philip A. Rovner (#3215)
Potter Anderson & Corroon LLP
Hercules Plaza, 6th Floor
P. O. Box 951
Wilmington, DE 19899
(302) 984-6000
provner@potteranderson.com

846666

Exhibit A

US007176489B2

(12) **United States Patent**
Ahn et al.

(10) **Patent No.: US 7,176,489 B2**
(45) **Date of Patent: *Feb. 13, 2007**

(54) **THIN-FILM TRANSISTOR AND METHOD OF MAKING SAME**

(75) Inventors: **Byung-Chul Ahn**, Kumi-shi (KR); **Hyun-Sik Seo**, Anyang-shi (KR)

(73) Assignee: **LG. Philips LCD. Co., Ltd.**, Seoul (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/872,527**

(22) Filed: **Jun. 22, 2004**

(65) **Prior Publication Data**

US 2004/0229413 A1 Nov. 18, 2004

Related U.S. Application Data

(60) Division of application No. 10/377,732, filed on Mar. 4, 2003, now Pat. No. 6,815,321, which is a division of application No. 10/154,955, filed on May 28, 2002, now Pat. No. 6,548,829, which is a continuation of application No. 09/940,504, filed on Aug. 29, 2001, now abandoned, which is a division of application No. 09/243,556, filed on Feb. 2, 1999, now Pat. No. 6,340,610, which is a division of application No. 08/918,119, filed on Aug. 27, 1997, now Pat. No. 5,905,274.

(30) **Foreign Application Priority Data**

Mar. 4, 1997 (KR) 97-07010

(51) **Int. Cl.**

H01L 29/04	(2006.01)
H01L 29/10	(2006.01)
H01L 31/036	(2006.01)
H01L 31/0376	(2006.01)
H01L 31/20	(2006.01)

(52) **U.S. Cl.** **257/59**; 257/57; 257/66; 257/72; 257/73; 257/291; 257/359

(58) **Field of Classification Search** 257/57, 257/59, 66, 73, 359, 72, 291
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,220,706 A 9/1980 Spak 430/318

(Continued)

FOREIGN PATENT DOCUMENTS

EP 0301571 2/1989

(Continued)

OTHER PUBLICATIONS

"Low Cost, High Display Quality TFT-LCD Process", Society for Information Display, EuroDisplay 96, Proceedings of the 16th International Display Research Conference, Oct. 1, 1996, 591-594.

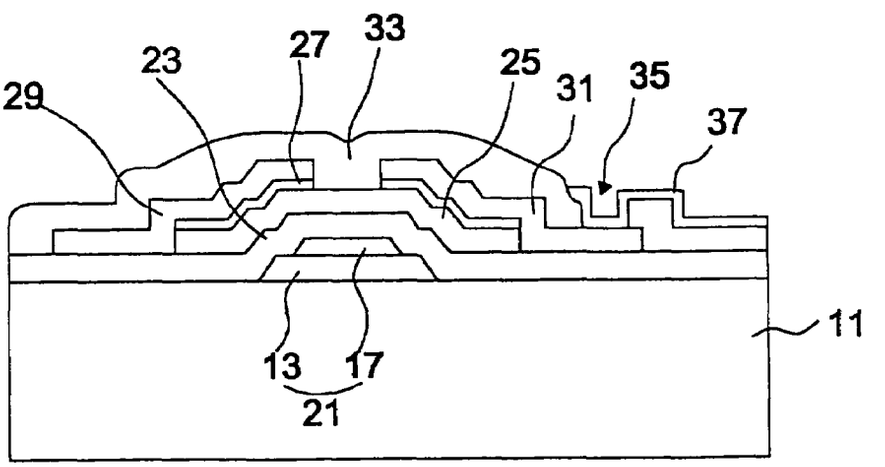
(Continued)

Primary Examiner—Ida M. Soward
(74) *Attorney, Agent, or Firm*—Birch, Stewart, Kolasch and Birch, LLP

(57) **ABSTRACT**

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by 1 to 4 μm. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

3 Claims, 6 Drawing Sheets



U.S. PATENT DOCUMENTS

5,036,370	A		7/1991	Miyago et al. 257/72
5,132,745	A		7/1992	Kwasnick et al. 257/412
5,156,986	A		10/1992	Wei et al. 438/159
5,162,933	A		11/1992	Kakuda et al. 349/46
5,191,453	A	*	3/1993	Okumura 349/47
5,349,205	A	*	9/1994	Kobayashi et al. 257/59
5,428,250	A		6/1995	Ikeda et al. 349/147
5,464,500	A		11/1995	Tsujimura et al. 216/34
5,644,146	A	*	7/1997	Arai et al. 257/66
5,686,749	A	*	11/1997	Matsuo 257/316
5,721,164	A	*	2/1998	Wu 438/159
5,731,216	A	*	3/1998	Holmberg et al. 438/30
5,808,336	A	*	9/1998	Miyawaki 257/315
5,808,595	A	*	9/1998	Kubota et al. 345/92
5,889,573	A	*	3/1999	Yamamoto et al. 349/152
5,903,326	A	*	5/1999	Lee 349/42
5,982,004	A	*	11/1999	Sin et al. 257/347
6,063,686	A	*	5/2000	Masuda et al. 438/406
6,201,281	B1	*	3/2001	Miyazaki et al. 257/347
6,333,518	B1	*	12/2001	Seo 257/72
2002/0048861	A1	*	4/2002	Seo 438/149

FOREIGN PATENT DOCUMENTS

EP	9206497	4/1992
EP	0602315	7/1993
EP	0812012	12/1997
GB	2253742	9/1992
GB	2254187	9/1992
GB	2307597	5/1997
JP	4097531	3/1982
JP	1120068	5/1989
JP	1222448	9/1989
JP	3114028	5/1991
JP	5315615	11/1993
JP	5343683	12/1993
JP	637311	2/1994
JP	6104241	4/1994
JP	06281954	10/1994
JP	7077695	3/1995
JP	08095083 A *	4/1996
JP	8254680	10/1996
KR	954593	2/1995
WO	9206504	4/1992

OTHER PUBLICATIONS

"Hilllock-Free Al-Gate Materials Using Stress-Absorbing Buffer Layer for Large Area AMLCDs" Society for information Display 96 Digest, pp. 341-344, 1996.

"Wet Etchant for Molybdenum Having High Selectivity Against Aluminum", IBM Technical Disclosure Bulletin, vol. 35, No. 3, Aug. 1, 1992, pp. 205-206, XP 000326238.

AT Patent Abstracts of Japan, vol. 9, No. 315 [E-365] and Japan 60-149173 (Hitachi).

AU Patent Abstracts of Japan, vol. 5, No. 197 [E-86] and Japan 56-118370 (Cho Lsi Gijutsu).

"Pure Al and Al-Alloy Gate-Line Processes in TFT-LCDs", Samsung Electronics Co., Ltd., Kiheung, Korea, C.W. Kim et al., SID 96 Digest, pp. 337-340.

* cited by examiner

FIG.1A

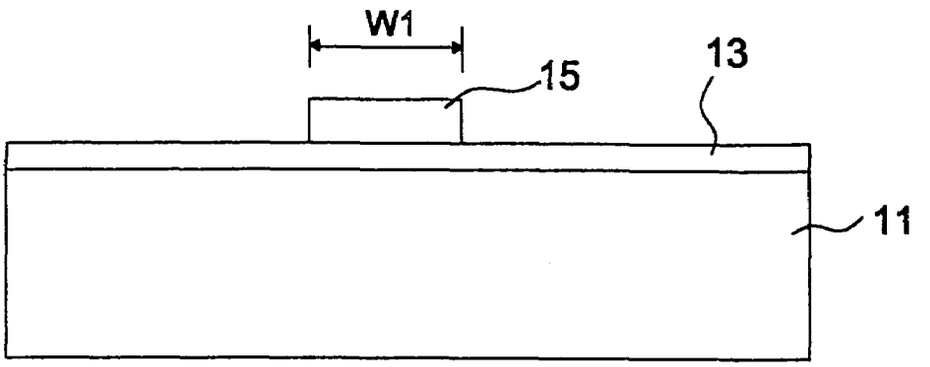


FIG.1B

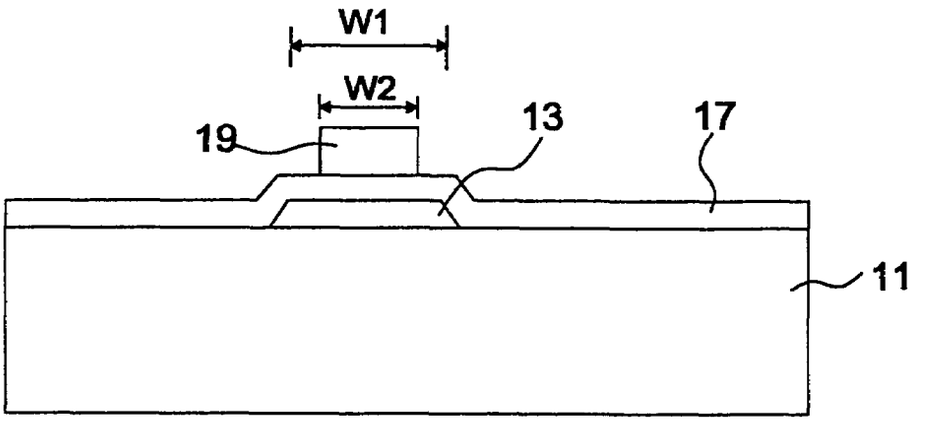


FIG.1C

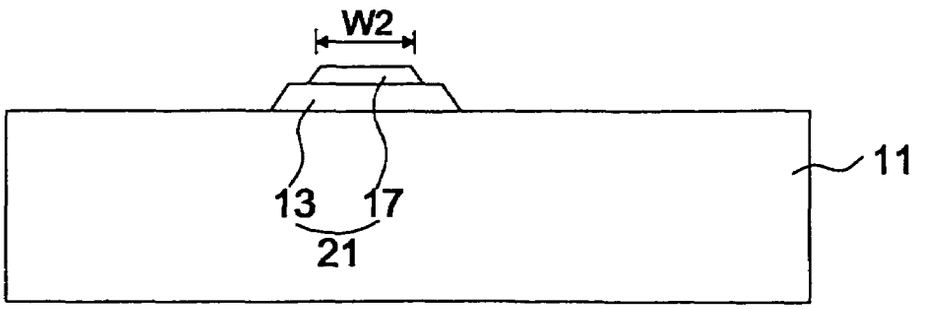


FIG.1D

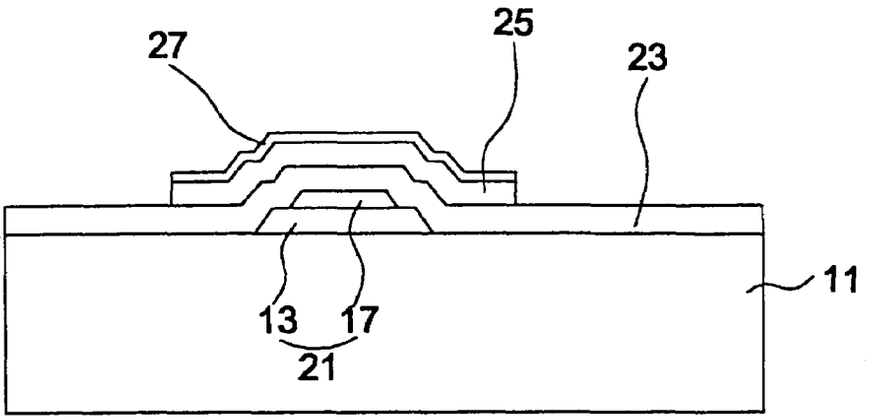


FIG.1E

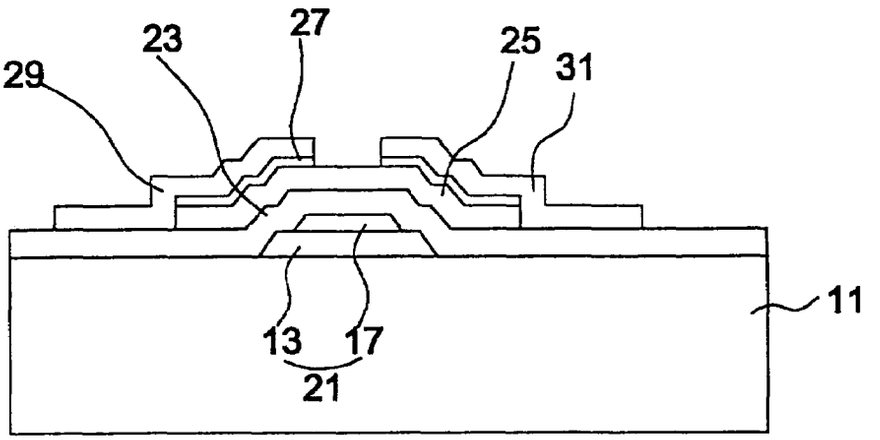


FIG.1F

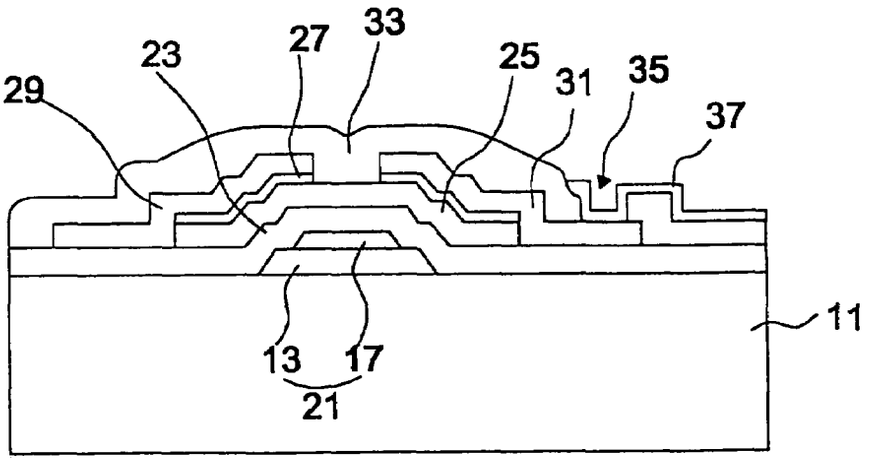


FIG.2

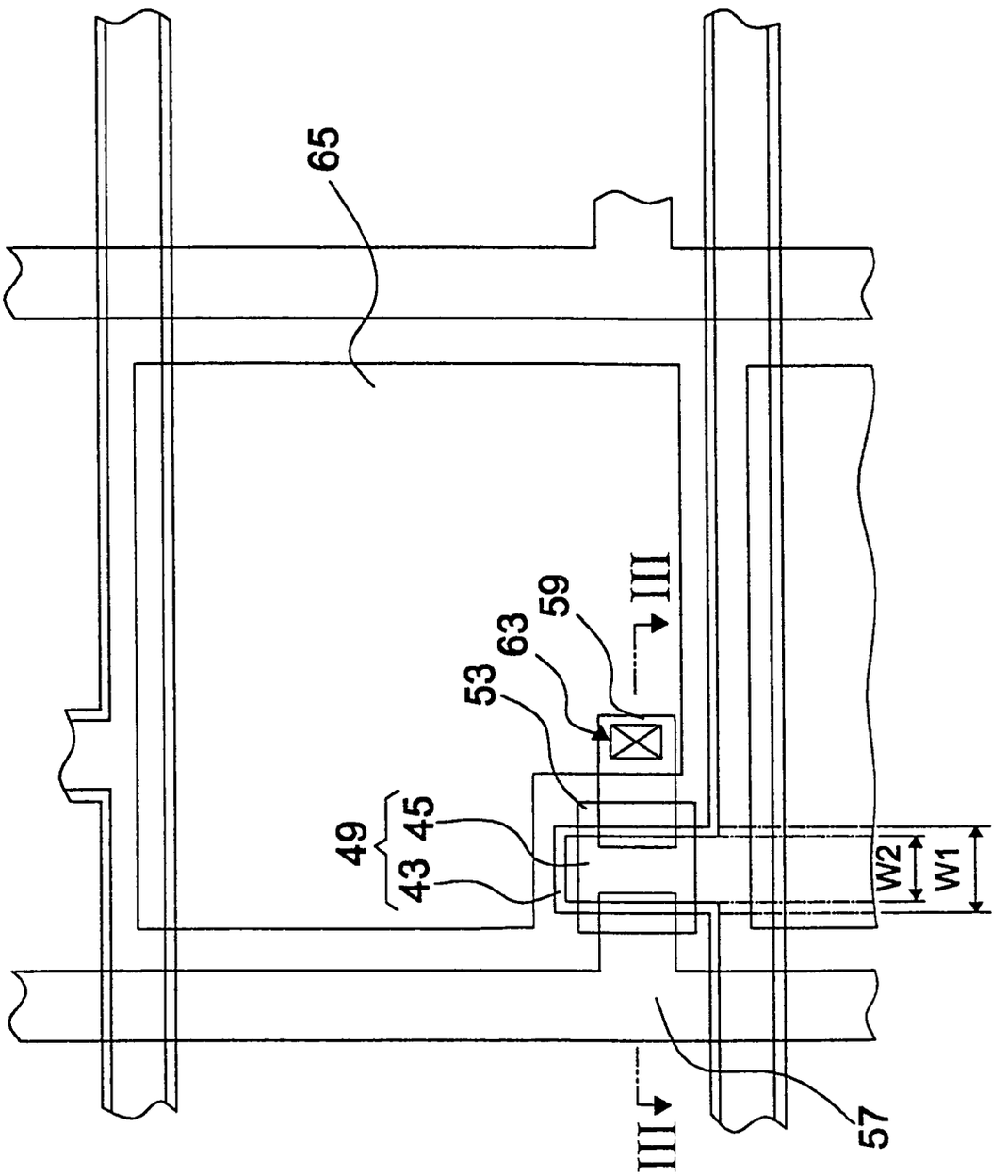


FIG.3

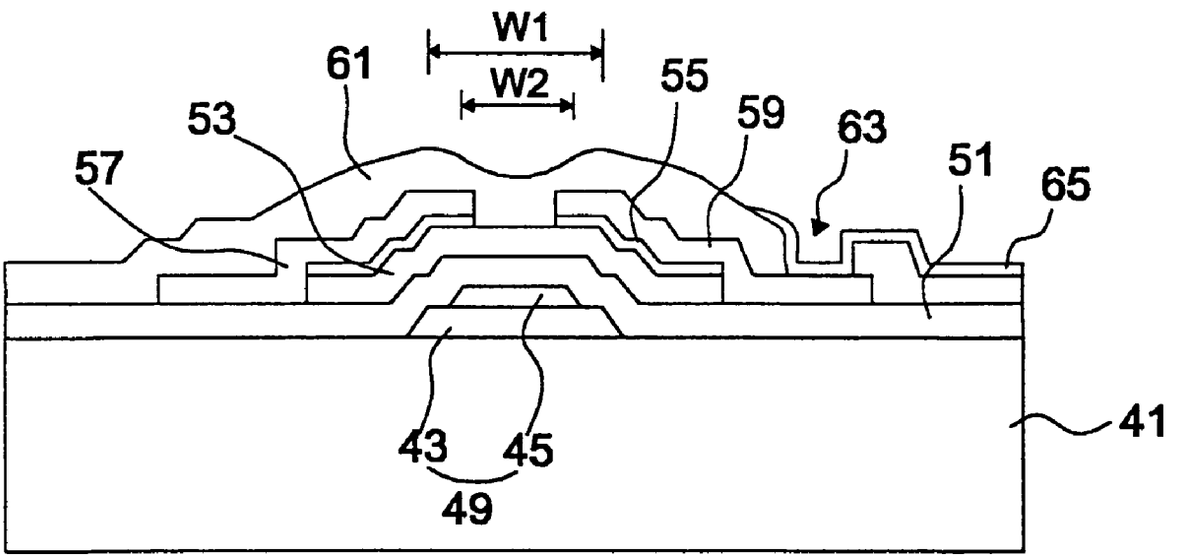


FIG.4A

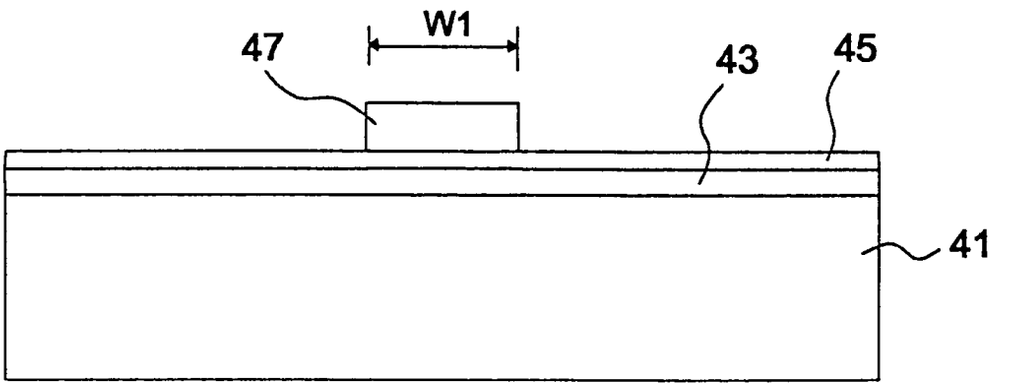


FIG.4B

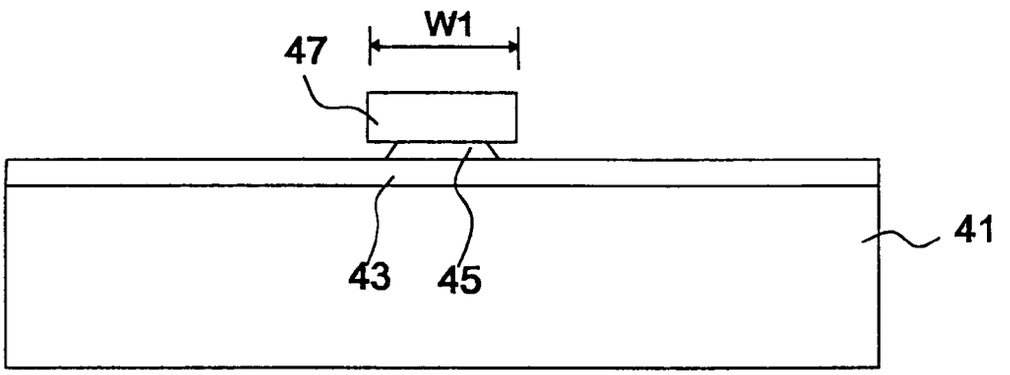


FIG.4C

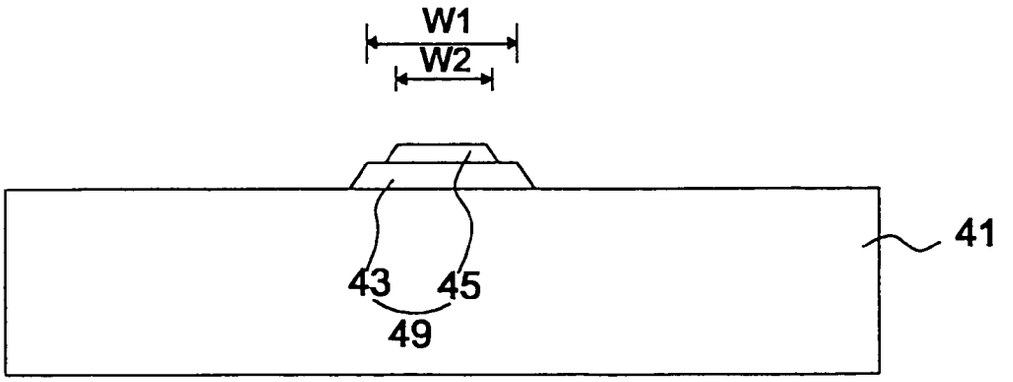


FIG.4D

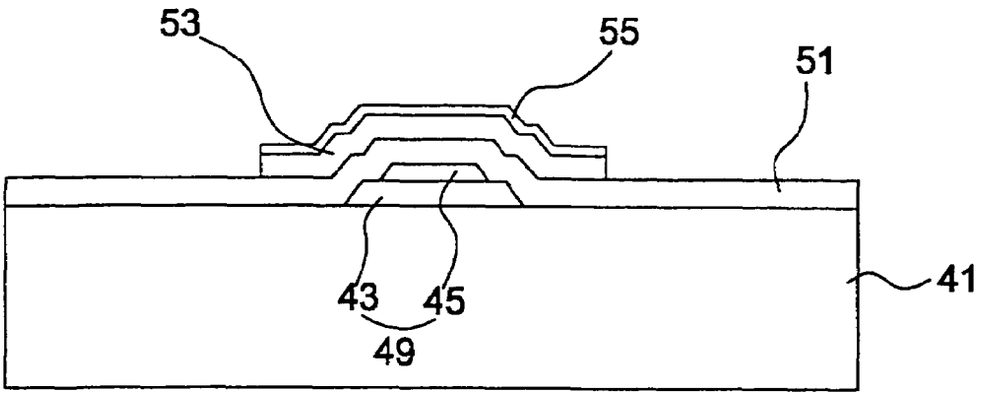


FIG.4E

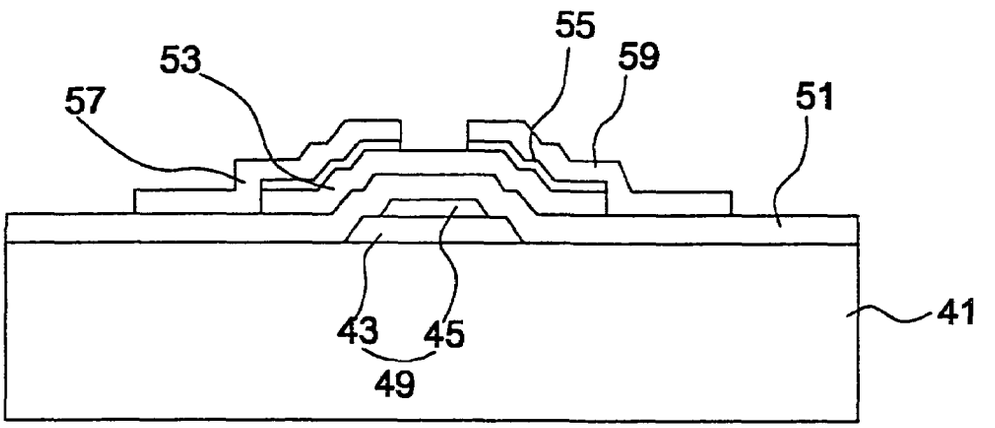
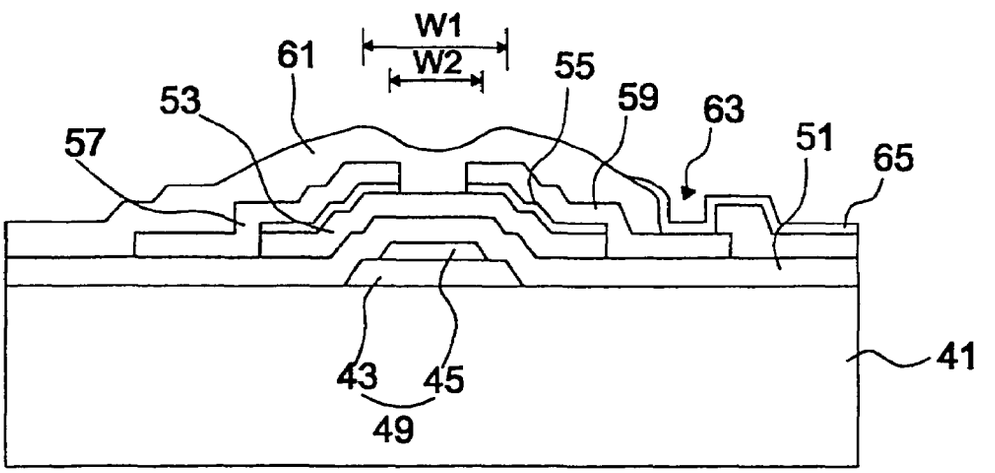


FIG.4F



THIN-FILM TRANSISTOR AND METHOD OF MAKING SAME

This application is a divisional of application Ser. No. 10/377,732 filed on Mar. 4, 2003 now U.S. Pat. No. 6,815,321, which is a divisional of application Ser. No. 10/154,955 filed on May 28, 2002 now U.S. Pat. No. 6,548,829, which is a continuation of abandoned application Ser. No. 09/940,504, filed on Aug. 29, 2001, which is a divisional application under 37 C.F.R. § 1.53(b) of patented prior application Ser. No. 09/243,556 (U.S. Pat. No. 6,340,610 B1) filed on Feb. 2, 1999 (Issued on Jan. 22, 2002), which is a divisional application under 37 C.F.R. § 1.53(b) of patented prior application Ser. No. 08/918,119 (U.S. Pat. No. 5,905,274) filed on Aug. 27, 1997 (Issued on May 18, 1999), the entire contents of which are hereby incorporated by reference and for which priority is claimed under 35 U.S.C. § 120; and this application claims priority of Application No. 97-07010 filed in Korea on Mar. 4, 1997 under 35 U.S.C. § 119.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a thin-film transistor of a liquid crystal display and, more particularly, to a thin-film transistor having a gate including a double-layered metal structure and a method of making such a double-layered metal gate.

2. Discussion of Related Art

An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electrodes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

The gate of the thin-film transistor is made of aluminum to reduce its wiring resistance, but an aluminum gate may cause defects such as hillock.

A double-layered metal gate, i.e., molybdenum-coated aluminum gate is considered as a substitute for the aluminum gate to overcome the problem of the hillock.

To fabricate a double-layered gate, metals such as aluminum and molybdenum are sequentially deposited, followed by a patterning process carried out via photolithography to form resulting metal films which have the same width. Although the double-layered gate is desirable to overcome the problem of hillock, the resulting deposited metal films forming the double-layered gate are so thick that a severe single step is created by a thickness difference between the metal films and a substrate, thereby causing a single step difference between the substrate and the double-layered gate which deteriorates the step coverage of a later formed gate oxide layer. The source and drain regions formed on the gate oxide layer may have disconnections between areas of the source and drain regions which are overlapped and non-overlapped with the gate, or electrically exhibit short circuits as a result of contact with the gate.

According to another method of forming the gate, each of the metal layers of Al and Mo form a double step difference with the substrate so as to improve the step coverage of the gate oxide layer.

FIGS. **1**A through **1**F are diagrams illustrating the process for fabricating a thin-film transistor of a method which is related to the invention described and claimed in the present application. The method shown in FIGS. **1**A–**1**F is not believed to be published prior art but is merely a recently discovered method related to the invention described and claimed in the present application.

Referring to FIG. **1**A, aluminum is deposited on a substrate **11** to form a first metal layer **13**. A first photoresist **15** is deposited on the first metal layer **13**. The first photoresist **15** is exposed and developed so as to have a certain width w**1** extending along the first metal layer **13**.

Referring to FIG. **1**B, the first metal layer **13** is patterned via wet etching using the first photoresist **15** as a mask so that the first metal layer **13** has a certain width w**1**. After the first photoresist **15** is removed, a second metal layer **17** is formed by depositing Mo, Ta, or Co on the substrate **11** so as to cover the first metal layer **13**. A second photoresist **19** is then deposited on the second metal layer **17**. The second photoresist **19** is exposed and developed so as to have a certain width w**2** extending along the second metal layer **17** and located above the first metal layer **13**.

Referring to FIG. **1**C, the second metal layer **17** is patterned via a wet etching process using the second photoresist **19** as a mask such that the second metal layer **17** has a certain width w**2** which is narrower than the width w**1** of the first metal layer **13**. After formation of the gate **21**, the second photoresist **19** is removed.

Thus, the patterned first and second metal layers **13** and **17** form a gate **21** having a double-layered metal structure that provides double step difference between the double-layered metal gate structure **21** and the substrate **11**. The formation of the gate **21** as described above and shown in FIGS. **1**A–**1**F requires the use of two photoresists **15**, **19** and two photoresist steps.

In the gate **21**, shown in FIG. **1**C, the second metal layer **17** is preferably centrally located on the first metal layer **13**. Although there is no specific information available regarding a relationship of w**1** to w**2** of this related art method, based on their understanding of this related method resulting in the structure shown in FIG. **1**C, the inventors of the invention described and claimed in the present application assume that the width difference w**1**–w**2** between the first and second metal layers **13** and **17** is larger than or equal to 4 μm, that is, w**1**–w**2**≧4 μm.

Referring to FIG. **1**D, a first insulating layer **23** is formed by depositing silicon oxide SiO_2 or silicon nitride Si_3N_4 as a single-layered or double-layered structure on the gate **21** and substrate **11**. Semiconductor and ohmic contact layers **25** and **27** are formed by sequentially depositing undoped polycrystalline silicon and heavily doped silicon on the first insulating layer **23**. The semiconductor and ohmic contact layers **25** and **27** are patterned to expose the first insulating layer **23** by photolithography.

Referring to FIG. **1**E, conductive metal such as aluminum is laminated on the insulating and ohmic contact layers **23** and **27**. The conductive metal is patterned by photolithography so as to form source electrode **29** and a drain electrode **31**. A portion of the ohmic contact layer **27** exposed between the source and drain electrodes **29** and **31** is etched by using the source and drain electrodes **29** and **31** as masks.

Referring to FIG. **1**F, silicon oxide or silicon nitride is deposited on the entire surface of the structure to form a second insulating layer **33**. The second insulating layer **33** is etched to expose a designated portion of the drain electrode **31**, thus forming a contact hole **35**. By depositing transparent and conductive material on the second insulating layer **33** and patterning it via photolithography, a pixel electrode **37** is formed so as to be electrically connected to the drain electrode **31** through the contact hole **35**.

According to the method of fabricating a thin-film transistor as described above and shown in FIGS. **1**A–**1**F, respective first and second metal layers are formed through photolithography using different masks so as to form the

gate with a double-layered metal structure, resulting in double step differences between the gate and substrate.

As a result of the double step difference between the gate **21** and the substrate **11** shown in FIG. **1**C, a hillock often occurs on both side portions of the first metal layer **13** which have no portion of the second metal layer **17** deposited thereon when the first metal layer **13** is wider than the second metal layer **17** as in FIG. **1**C. Another problem with this related art method is that the process for forming a gate is complex and requires two photoresists **15**, **19** and two steps of deposition and photolithography. As a result, the contact resistance between the first and second metal layers may be increased.

Another related art method of forming a double metal layer gate structure is described in "Low Cost, High Quality TFT-LCD Process", SOCIETY FOR INFORMATION DISPLAY EURO DISPLAY 96, Proceedings of the 16th International Display Research Conference, Birmingham, England, Oct. 1, 1996, pages 591–594. One page 592 of this publication, a method of forming a double metal gate structure includes the process of depositing two metal layers first and then patterning the two metal layer to thereby eliminate an additional photoresist step. However, with this method, process difficulties during the one step photoresist process for forming the double metal layer gate resulted in the top layer being wider than the bottom layer causing an overhang condition in which the top layer overhangs the bottom layer. This difficulty may result in poor step coverage and disconnection. This problem was solved by using a three-step etching process in which the photoresist had to be baked before each of the three etching steps to avoid lift-off or removal of the photoresist during etching. This three-step etching process and required baking of the photoresist significantly increases the complexity and steps of the gate forming method.

SUMMARY OF THE INVENTION

To overcome the problems discussed above, the preferred embodiments of the present invention provide a thin-film transistor which prevents a hillock and deterioration of step coverage of a later formed gate oxide layer on a double metal layer gate.

The preferred embodiments of the present invention also provide a method of fabricating a thin-film transistor that simplifies the process for forming a double metal layer gate.

The preferred embodiments of the present invention further provide a method of fabricating a thin-film transistor that reduces the contact resistance between the first and second metal layers constituting a gate.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof, as well as, the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the preferred embodiments of the present invention, as embodied and broadly described, a thin-film transistor preferably comprises a substrate, and a gate including a double-layered structure of first and second metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μm, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a desired width on the second metal layer; patterning the second metal layer via an isotropic etching using the photoresist as a mask; patterning the first metal layer via an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have a desired width, thus forming a gate having a laminated structure of the first and second layers; and removing the photoresist.

These and other elements, features, and advantages of the preferred embodiments of the present invention will be apparent from the following detailed description of the preferred embodiments of the present invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate preferred embodiments of the invention and together with the description serve to explain the principles of the invention, in which:

FIGS. **1**A through **1**F are diagrams illustrating a process for fabricating a thin-film transistor according to a method of the related art;

FIG. **2** is a top view of a thin-film transistor according to a preferred embodiment of the present invention;

FIG. **3** is a cross-sectional view taken along line III—III of FIG. **2**; and

FIGS. **4**A through **4**F are diagrams illustrating a process for fabricating a thin-film transistor of preferred embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIG. **2** is a top view of a thin-film transistor according to a preferred embodiment of the present invention. FIG. **3** is a cross-sectional view taken along line III—III of FIG. **2**.

The thin-film transistor comprises a gate **49** having a double-layered structure of a first metal layer **43**, a second metal layer **45** disposed on a substrate **41**, a first insulating layer **51**, a second insulating layers **61**, a semiconductor layer **53**, an ohmic contact layer **55**, a source electrode **57**, a drain electrode **59**, and a pixel electrode **65**.

The gate **49** has a double-layered structure including the first and second metal layers **43** and **45** disposed on the substrate **41**. The first metal layer **43** is preferably formed from a conductive metal such as Al, Cu, or Au deposited to have a certain width w**1**. The second metal layer **45** is preferably formed from a refractory metal such as Mo, Ta, or Co deposited to have a certain width w**2**.

The present inventors have discovered that a relationship between the width of the first metal layer and the width of the second metal layer of a double metal layer gate electrode is critical to preventing deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate. More specifically, the present inventors determined that a structure wherein the first metal layer **43** is wider than the second metal layer **45** by about 1 to 4 μm, for example, 1 μm<w**1**−w**2**<4 μm, provides maximum prevention of dete-

rioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate.

To achieve the best results, the second metal layer **45** is preferably positioned substantially in the middle of the first metal layer **45**, so that both side portions of the first metal layer **43** which have no portion of the second metal layer **45** disposed thereon have substantially the same width as each other. The width of each of the side portions is preferably larger than about 0.5 μm but less than about 2 μm.

The first insulating layer **51** is preferably formed by depositing single layer of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the substrate including the gate **49**.

The semiconductor and ohmic contact layers **53** and **55** are formed on the portion of the first insulating layer **51** corresponding to the gate **49** by sequentially depositing undoped amorphous silicon and heavily doped amorphous silicon and patterning the two silicon layers. The semiconductor layer **53** is used as the active region of an element, thus forming a channel by means of a voltage applied to the gate **49**. The ohmic contact layer **55** provides an ohmic contact between the semiconductor layer **53** and the source and drain electrodes **57** and **59**. The ohmic contact layer **55** is not formed in the portion that becomes the channel of the semiconductor layer **53**.

The source and drain electrodes **57** and **59** are in contact with the ohmic contact layer **55**, and each electrode **57**, **59** extends to a designated portion on the first insulating layer **51**.

The second insulating layer **61** is formed by depositing insulating material such as silicon oxide SiO_2 silicon nitride Si_3N_4 to cover the source and drain electrodes **57** and **59** and the first insulating layer **51**. The second insulating layer **61** on the drain electrode **59** is removed to form a contact hole **63**. The pixel electrode **65** is formed from transparent and conductive material such as ITO (Indium Tin Oxide) or Tin oxide SnO_2, so that it is connected to the drain electrode **59** through the contact hole **63**.

In the first and second metal layers **43** and **45** constituting the gate **49**, each side portion of the first metal layer **43** having no portion of the second metal layer **45** thereon has a width that is preferably larger than about 0.5 μm and less than about 2 μm. Because the first metal layer **43** is wider than the second metal layer **45** by about 1.0 μm to 4.0 μm, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate **49** and substrate **41**. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer **51** which deterioration occurs in prior art devices. The hillock in the first metal layer **43** is also avoidable because the width difference between the first and second metal layers **43** and **45** is between about 1 μm to 4 μm.

FIGS. **4**A through **4**F are diagrams illustrating the process for fabricating the thin-film transistor of the preferred embodiments of the present invention.

Referring to FIG. **4**A, metal such as Al, Cu, or Au is deposited on a substrate so as to form a first metal layer **43**. A second metal layer **45** is formed from Mo, Ta, or Co and deposited on the first metal layer **43** without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers **43** and **45** are sequentially deposited so as to preferably have a thickness as large as about 500–4000 Angstroms and 500–2000 Angstroms, respectively, by means of sputtering or chemical vapor deposition (hereinafter, referred to as CVD) without breaking a vacuum state. As a result, the contact resistance between the first and second metal layers **43** and **45** is reduced.

According to the preferred embodiments of the present invention, a single photoresist step is used to pattern both the first metal layer **43** and the second metal layer **45** simultaneously. In the single photoresist step, a photoresist **47** is deposited on the second metal layer **45** and then the photoresist **47** is patterned through exposure and development to have the width w**1** on a designated portion of the second metal layer **45**.

Referring to FIG. **4**B, the second metal layer **45** is patterned with an etching solution preferably prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3, by means of a wet etching using the photoresist **47** as a mask. Because the portion of the second metal layer **45** covered with the photoresist **47**, as well as, exposed side portions of the second metal layer **45** are isotropically etched, the second metal layer **45** is preferably patterned to have the width w**2** which is narrower than the width w**1** of the photoresist **47** which is the same as the width w**1** of the first metal layer **43**, that is, about 1 μm<w**1**−w**2**<4 μm. Each side portion of the second metal layer **45** preferably has a width larger than about 0.5 μm and less than about 2 μm. That is, the two side portions of the second metal layer **45** covered with the photoresist **47** are preferably etched to have substantially the same width as each other. The lateral surfaces of the second metal layer **45** are preferably etched to have a substantially rectangular or inclined shape.

Referring to FIG. **4**C, the first metal layer **43** is patterned via dry etching having anisotropic etching characteristic such as reactive ion etching (hereinafter, referred to as RIE) by using the photoresist **47** as a mask. When etching the first metal layer **43** other than the portion of the layer **43** covered with the photoresist **47**, the first metal layer **43** preferably has the same width w**1** of the photoresist **47**. Thus, patterning of the first and second metal layers **43**, **45**, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the relation between the first and second metal layers **43** and **45** also may be represented by about 1 μm<w**1**−w**2**<4 μm.

The first and second metal layers **43** and **45** resulting form the single photoresist step process described above form a gate **49** having a double-layered metal structure. The gate **49** has the second metal layer **45** positioned substantially in the middle of the first metal layer **43** so that the each side portion of the first metal layer **43** having no second metal layer **45** thereon is wider than about 0.5 μm but narrower than about 2 μm. The photoresist **47** remaining on the second metal layer **45** is removed after the two etching steps are completed.

Referring to FIG. **4**D, a first insulating layer **51** is formed by depositing a single layer or double layers of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the gate **49** and substrate **41** by CVD. Because each side portion of the first metal layer **43** having no second metal layer **45** thereon is wider than 0.5 μm, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer **51** from being deteriorated as in prior art devices. The hillock in the first metal layer **43** is also avoidable because a width of a portion of the first metal layer **43** which is exposed is less than about 2 μm.

Amorphous silicon which is undoped and heavily doped amorphous silicon are sequentially deposited on the first

insulating layer **41** by CVD, thus forming semiconductor and ohmic contact layers **53** and **55**. The ohmic contact and semiconductor layers **55** and **53** are patterned by means of photolithography to expose the first insulating layer **51**.

Referring to FIG. **4**E, conductive metal such as Al or Cr is laminated on the insulating and ohmic contact layers **51** and **55** and patterned by photolithography to form source and drain electrodes **57** and **59**. The ohmic contact layer **55** exposed between the source and drain electrodes **57** and **59** is etched by using the source drain electrodes **57** and **59** as masks.

Referring to FIG. **4**F, a second insulating layer **61** is formed by depositing insulating material such as silicon oxide or silicon nitride by CVD on the entire surface of the above structure. The second insulating layer is removed by photolithography to expose a designated portion of the drain electrode **59** and thus form a contact hole **63**. Once transparent and conductive material such as ITO (Indium Tin Oxide) or Tin oxide SnO_2 is deposited on the second insulating layer **61** via sputtering and patterned by photolithography, a pixel electrode **65** is formed so that it is electrically connected to the drain electrode **59** through the contact hole **63**.

In another preferred embodiment of the present invention, the first and second metal layers **43** and **45** are first etched by means of a dry etching having anisotropic etching characteristic such as RIE by using the photoresist **47** as a mask. The gate **49** is formed by etching the second metal layer **45** under the photoresist **47** with an etching solution prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3.

In still another preferred embodiment of the present invention, the gate **49** is formed through a single etching step process for etching the first and second metal layers **43** and **45** simultaneously and via a single etching step, where the second metal layer **45** is etched more quickly than the first metal layer **43** with an etching solution prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3. Because of the etching material and metals used for the first and second metal layers of the gate, only a single etching step is required. Despite the fact that a single etching step is used, it is still possible to obtain the relationship between the widths w**1** and w**2** of the first and second metal layers described above. In this process, the first and second metal layers forming the gate **49** are formed and patterned with a single photo resist step as described above and a single etching step.

As described above, in the preferred embodiments of the present invention, the first and second metal layers are sequentially deposited on the substrate without performing a masking step between the step of depositing the first metal layer and the second metal layer, followed by forming a photoresist that covers a designated portion of the second metal layer. In one preferred embodiment, the second metal layer is wet etched by using the photoresist as a mask but the first metal layer is dry etched. As a result, the double-metal gate is formed. In another preferred embodiment, a single etching step is used to form the double-metal gate wherein both the first metal layer and the second metal layer are wet etched, but the difference in etching rates of the first and second metal layers produces different etching affects which result in the desired double-step structure.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A thin film transistor comprising:

a substrate; and

a double-layered metal gate having a first metal layer and a second metal layer thereon, a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 μm.

2. The transistor of claim **1**, wherein the first metal layer has a first and second side portion being exposed from the second metal layer, each side portion being at least about 0.5 μm in width.

3. The transistor of claim **2**, wherein each side portion of the first metal layer is less than about 2 μm in width.

* * * * *

Exhibit B

US006815321B2

(12) **United States Patent**
Ahn et al.

(10) **Patent No.: US 6,815,321 B2**
(45) **Date of Patent: Nov. 9, 2004**

(54) **THIN-FILM TRANSISTOR AND METHOD OF MAKING SAME**

(75) Inventors: **Byung-Chul Ahn**, Kumi-shi (KR); **Hyun-Sik Seo**, Anyang-shi (KR)

(73) Assignee: **LG. Philips LCD Co., Ltd.**, Seoul (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/377,732**

(22) Filed: **Mar. 4, 2003**

(65) **Prior Publication Data**

US 2003/0164520 A1 Sep. 4, 2003

Related U.S. Application Data

(62) Division of application No. 10/154,955, filed on May 28, 2002, now Pat. No. 6,548,829, which is a continuation of application No. 09/940,504, filed on Aug. 29, 2001, now abandoned, which is a division of application No. 09/243,556, filed on Feb. 2, 1999, now Pat. No. 6,340,610, which is a division of application No. 08/918,119, filed on Aug. 27, 1997, now Pat. No. 5,905,274.

(30) **Foreign Application Priority Data**

Mar. 4, 1997 (KR) 1997-7010

(51) **Int. Cl.**[7] **H01L 21/3205**

(52) **U.S. Cl.** **438/592**; 438/155; 438/481; 438/482; 438/483; 438/588

(58) **Field of Search** 257/149, 158, 257/482, 588, 592

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,220,706 A		9/1980	Spak	
5,036,370 A		7/1991	Miyago et al.	
5,132,745 A	*	7/1992	Kwasnick et al.	257/412
5,156,986 A		10/1992	Wei et al.	
5,162,933 A		11/1992	Kakuda et al.	
5,428,250 A		6/1995	Ikeda et al.	
5,464,500 A		11/1995	Tsujimura et al.	
5,821,159 A	*	10/1998	Ukita	438/592
6,340,610 B1	*	1/2002	Ahn et al.	438/158

FOREIGN PATENT DOCUMENTS

EP	0301571	2/1989
EP	9206497	4/1992
EP	0602315	7/1993
EP	0812012	12/1997

(List continued on next page.)

OTHER PUBLICATIONS

"Low Cost, High Display Quality TFT–LCD Process", Society for Information Display, EuroDisplay 96, Proceedings of the 16th International Display Research Conference, Oct. 1, 1996, 591–594.

"Hilllock–Free Al–Gate Materials Using Stress–Absorbing Buffer Layer for Large Area AMLCDs" Society for information Display 96 Digest, pp. 341–344, 1996.

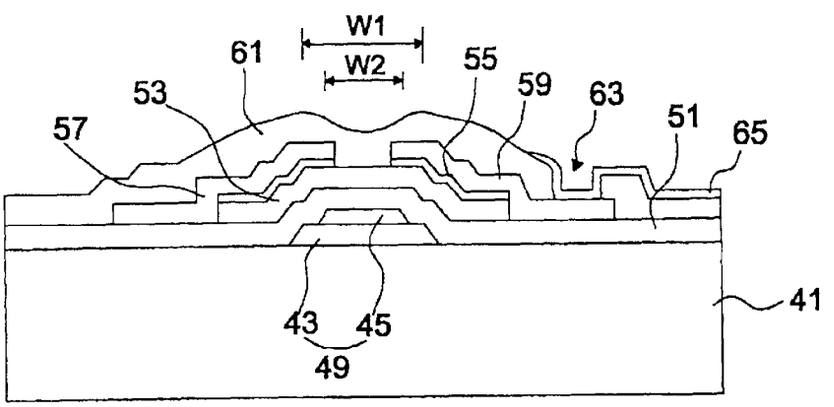
(List continued on next page.)

Primary Examiner—Long Pham
Assistant Examiner—Wai-Sing Louie
(74) *Attorney, Agent, or Firm*—Birch, Stewart, Kolasch & Birch, LLP

(57) **ABSTRACT**

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by 1 to 4 μm. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

22 Claims, 6 Drawing Sheets



FOREIGN PATENT DOCUMENTS

GB	2253742	9/1992
GB	2254187	9/1992
GB	2307597	5/1997
JP	4097531	3/1982
JP	1120068	5/1989
JP	1222448	9/1989
JP	3114028	5/1991
JP	5315615	11/1993
JP	5343683	12/1993
JP	637311	2/1994
JP	6104241	4/1994
JP	06281954	10/1994
JP	7077695	3/1995
JP	8254680	10/1996
KR	954593	2/1995
WO	9206504	4/1992

OTHER PUBLICATIONS

"Wet Etchant for Molybdenum Having High Selectivity Against Aluminum", IBM Technical Disclosure Bulletin, vol. 35, No. 3, Aug. 1, 1992, pp. 205–206, XP 000326238.
AT Patent Abstracts of Japan, vol. 9, No. 315 [E–365] and Japan 60–149173 (Hitachi).
AU Patent Abstracts of Japan, vol. 5, No. 197 [E–86] and Japan 56–118370 (Cho Lsi Gijutsu).
"Pure Al and Al–Alloy Gate–Line Processes in TFT–L-CDs", Samsung Electronics Co., Ltd., Kiheung, Korea, C.W. Kim et al., SID 96 Digest, pp. 337–340.

* cited by examiner

FIG.1A

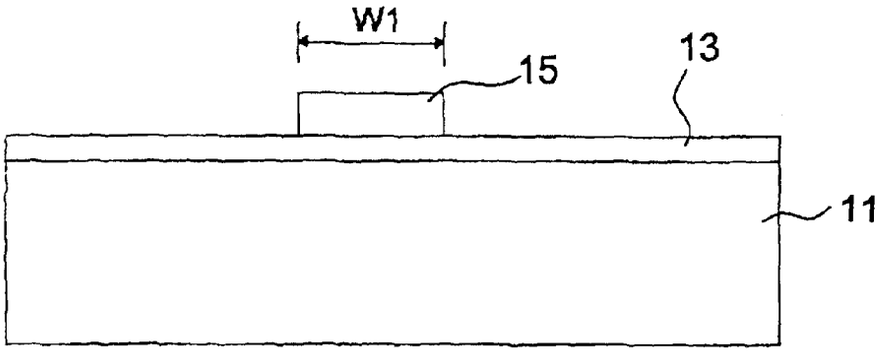


FIG.1B

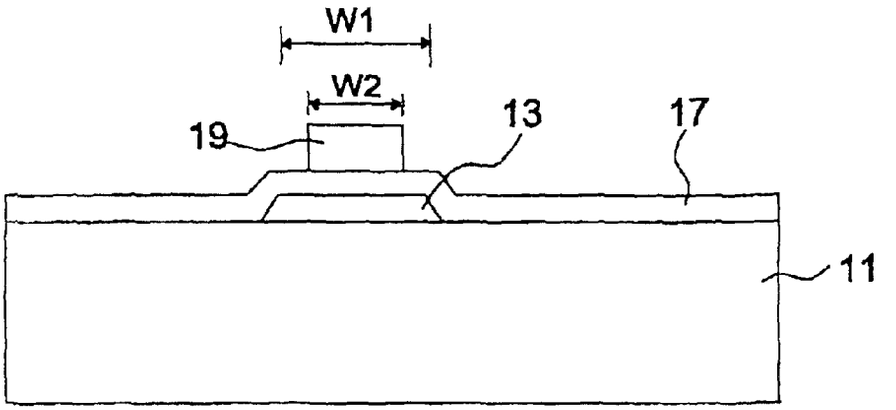


FIG.1C

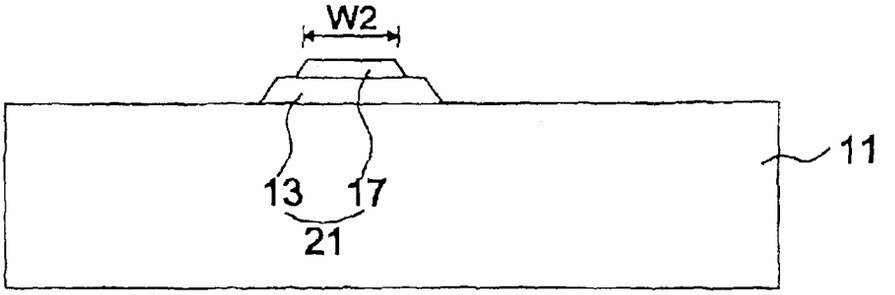


FIG.1D

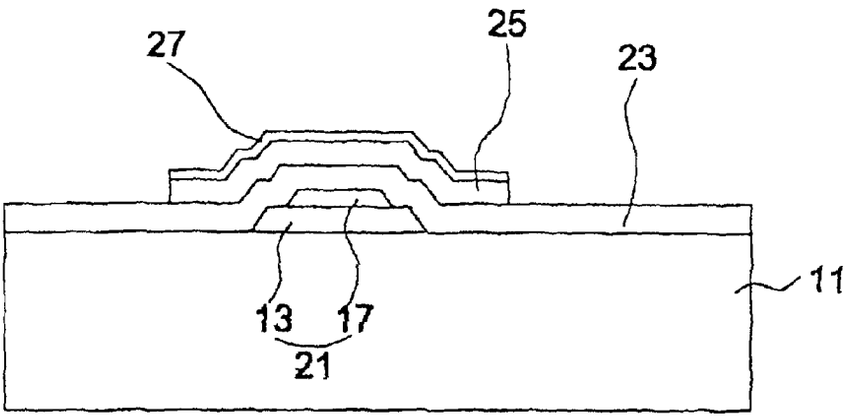


FIG.1E

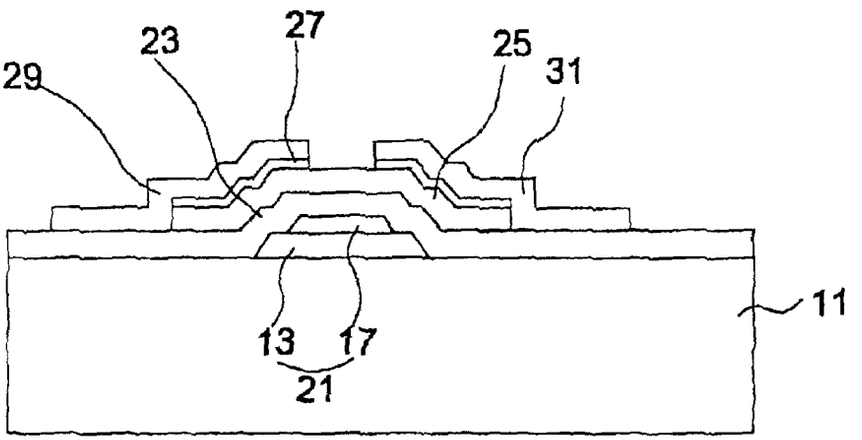


FIG.1F

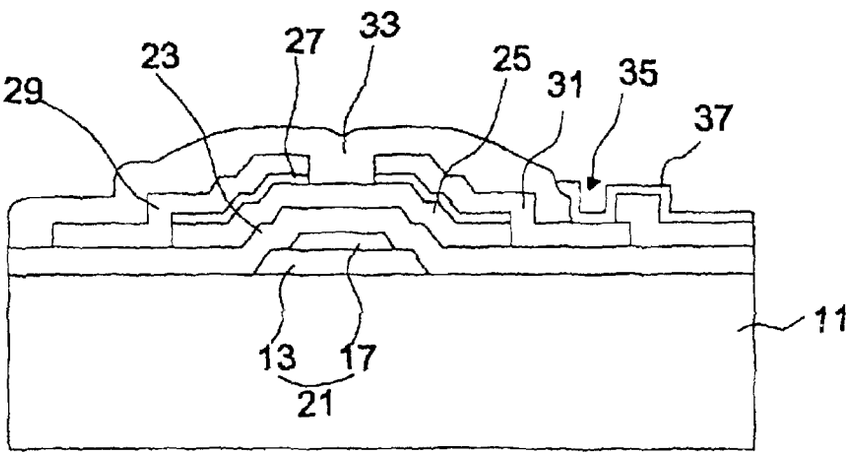


FIG.2

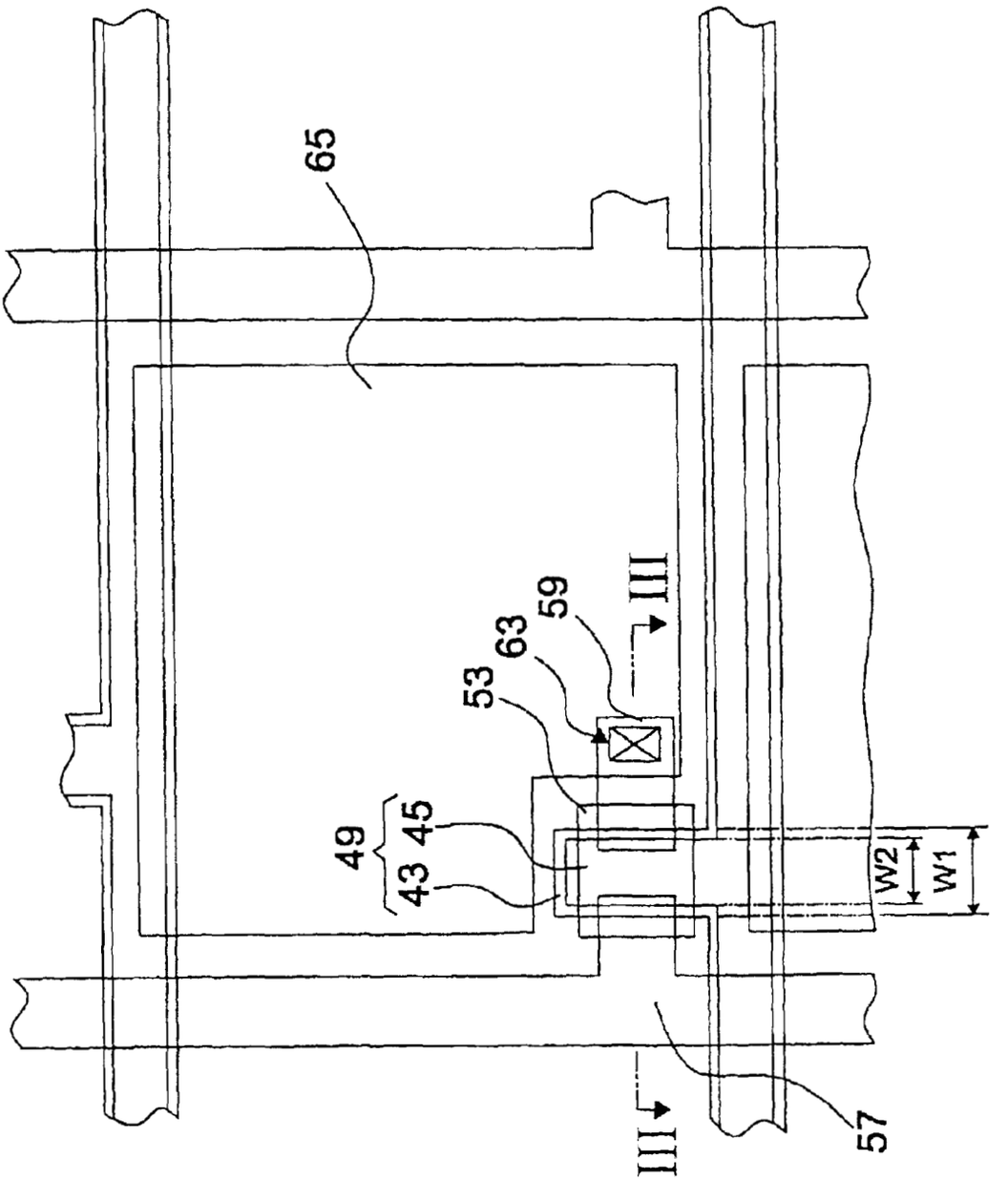


FIG.3

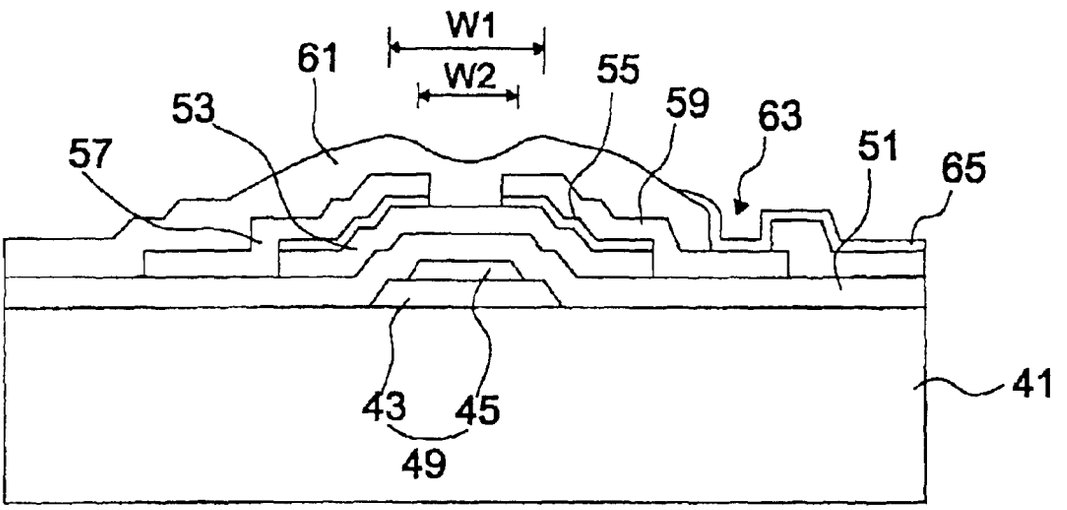


FIG.4A

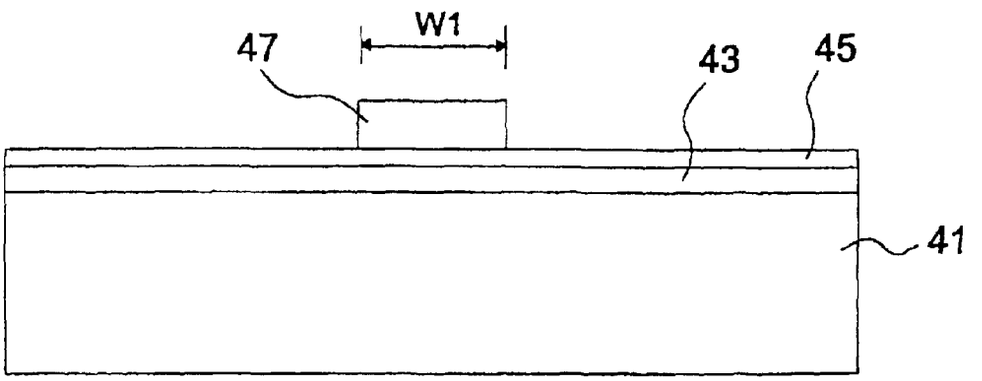


FIG.4B

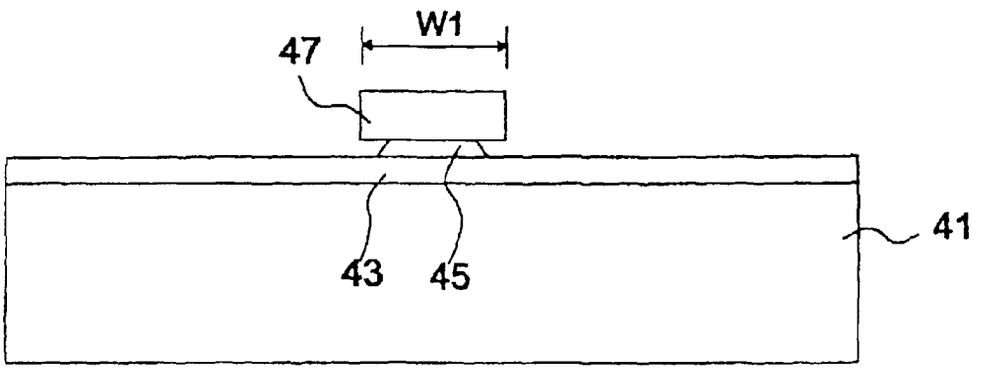


FIG.4C

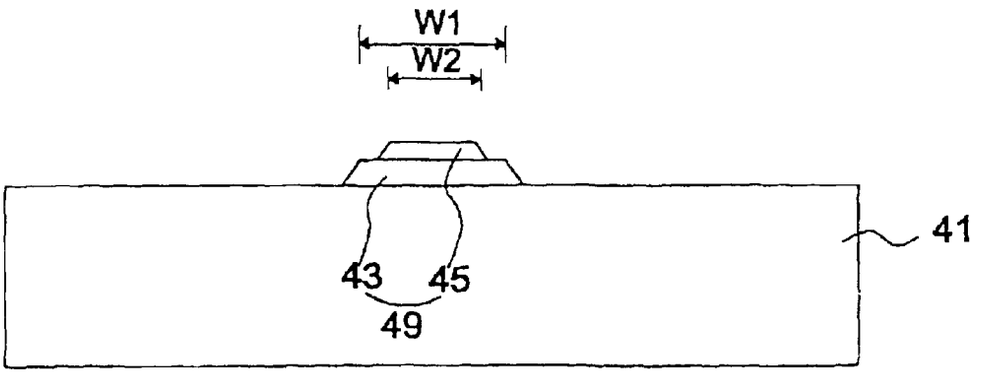


FIG.4D

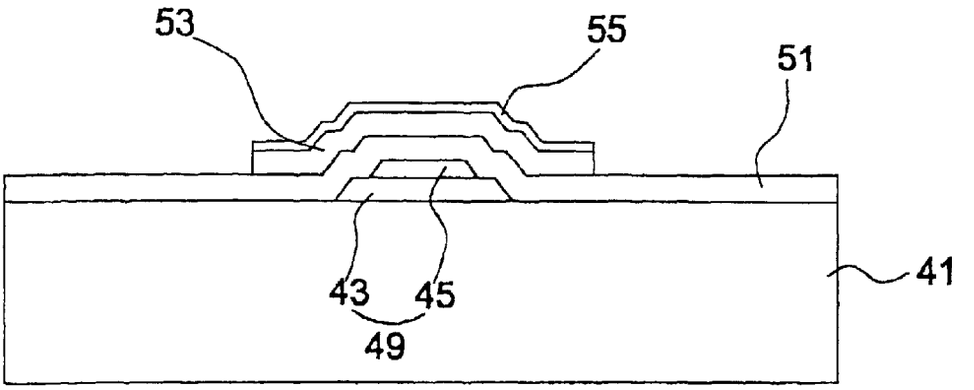


FIG.4E

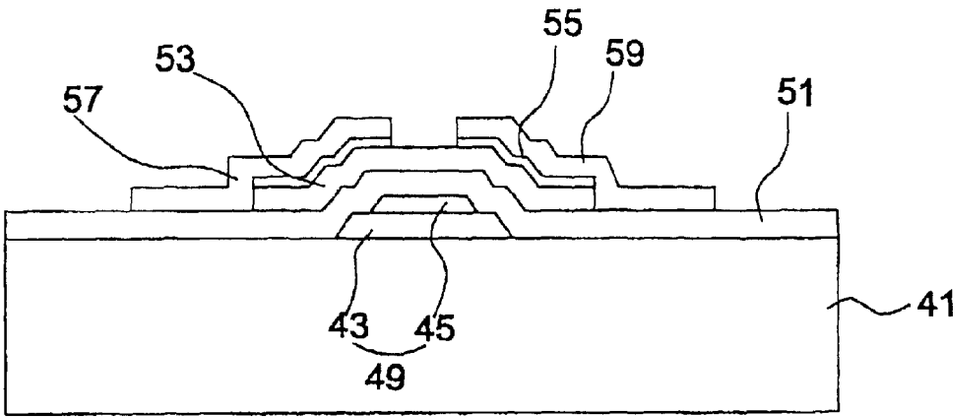
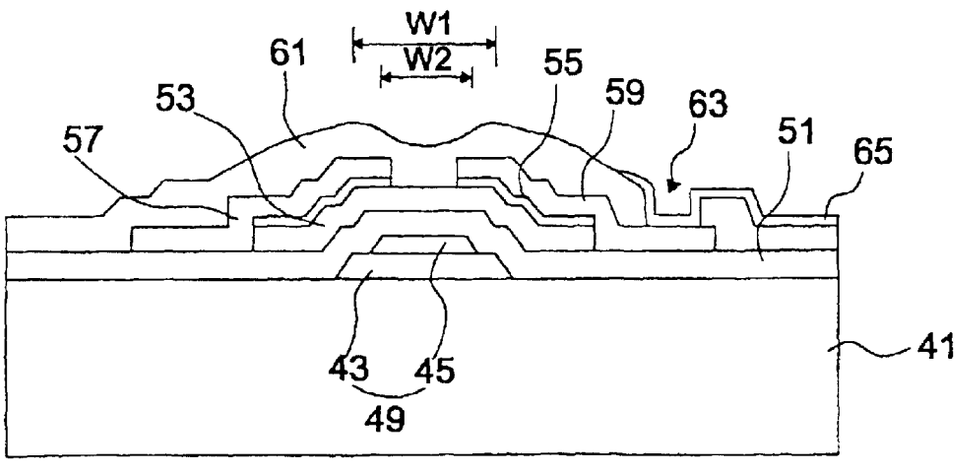


FIG.4F



THIN-FILM TRANSISTOR AND METHOD OF MAKING SAME

This application is a divisional of application Ser. No. 10/154,955, filed on May 28, 2002, now U.S. Pat. No. 6,548,829 which is a continuation of abandoned application Ser. No. 09/940,504, filed on Aug. 29, 2001, which is a divisional application under 37 C.F.R. §1.53(b) of patented prior application Ser. No. 09/243,556 (U.S. Pat. No. 6,340,610 B1) filed on Feb. 2, 1999 (Issued on Jan. 22, 2002):, which is divisional application under 37 C.F.R. §1.53(b) of patented prior application Ser. No. 08/918,119 (U.S. Pat. No. 5,905,274) filed on Aug. 27, 1997 (Issued on May 18, 1999) the entire contents of which are hereby incorporated by reference and for which priority is claimed under 35 U.S.C. §120; and this application claims priority of Application No. 97-07010 filed in Korea on Mar. 4, 1997 under 35 U.S.C. §119.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a thin-film transistor of a liquid crystal display and, more particularly, to a thin-film transistor having a gate including a double-layered metal structure and a method of making such a double-layered metal gate.

2. Discussion of Related Art

An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electrodes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

The gate of the thin-film transistor is made of aluminum to reduce its wiring resistance, but an aluminum gate may cause defects such as hillock.

A double-layered metal gate, i.e., molybdenum-coated aluminum gate is considered as a substitute for the aluminum gate to overcome the problem of the hillock.

To fabricate a double-layered gate, metals such as aluminum and molybdenum are sequentially deposited, followed by a patterning process carried out via photolithography to form resulting metal films which have the same width. Although the double-layered gate is desirable to overcome the problem of hillock, the resulting deposited metal films forming the double-layered gate are so thick that a severe single step is created by a thickness difference between the metal films and a substrate, thereby causing a single step difference between the substrate and the double-layered gate which deteriorates the step coverage of a later formed gate oxide layer. The source and drain regions formed on the gate oxide layer may have disconnections between areas of the source and drain regions which are overlapped and non-overlapped with the gate, or electrically exhibit short circuits as a result of contact with the gate.

According to another method of forming the gate, each of the metal layers of Al and Mo form a double step difference with the substrate so as to improve the step coverage of the gate oxide layer.

FIGS. **1A** through **1F** are diagrams illustrating the process for fabricating a thin-film transistor of a method which is related to the invention described and claimed in the present application. The method shown in FIGS. **1A–1F** is not believed to be published prior art but is merely a recently discovered method related to the invention described and claimed in the present application.

Referring to FIG. **1A**, aluminum is deposited on a substrate **11** to form a first metal layer **13**. A first photoresist **15** is deposited on the first metal layer **13**. The first photoresist **15** is exposed and developed so as to have a certain width w1 extending along the first metal layer **13**.

Referring to FIG. **1B**, the first metal layer **13** is patterned via wet etching using the first photoresist **15** as a mask so that the first metal layer **13** has a certain width w1. After the first photoresist **15** is removed, a second metal layer **17** is formed by depositing Mo, Ta, or Co on the substrate **11** so as to cover the first metal layer **13**. A second photoresist **19** is then deposited on the second metal layer **17**. The second photoresist **19** is exposed and developed so as to have a certain width w2 extending along the second metal layer **17** and located above the first metal layer **13**.

Referring to FIG. **1C**, the second metal layer **17** is patterned via a wet etching process using the second photoresist **19** as a mask such that the second metal layer **17** has a certain width w2 which is narrower than the width w1 of the first metal layer **13**. After formation of the gate **21**, the second photoresist **19** is removed.

Thus, the patterned first and second metal layers **13** and **17** form a gate **21** having a double-layered metal structure that provides double step difference between the double-layered metal gate structure **21** and the substrate **11**. The formation of the gate **21** as described above and shown in FIGS. **1A–1F** requires the use of two photoresists **15**, **19** and two photoresist steps.

In the gate **21**, shown in FIG. **1C**, the second metal layer **17** is preferably centrally located on the first metal layer **13**. Although there is no specific information available regarding a relationship of w1 to w2 of this related art method, based on their understanding of this related method resulting in the structure shown in FIG. **1C**, the inventors of the invention described and claimed in the present application assume that the width difference w1−w2 between the first and second metal layers **13** and **17** is larger than or equal to 4 μm, that is, $w1-w2 \geqq 4\ \mu m$.

Referring to FIG. **1D**, a first insulating layer **23** is formed by depositing silicon oxide SiO_2 or silicon nitride Si_3N_4 as a single-layered or double-layered structure on the gate **21** and substrate **11**. Semiconductor and ohmic contact layers **25** and **27** are formed by sequentially depositing undoped polycrystalline silicon and heavily doped silicon on the first insulating layer **23**. The semiconductor and ohmic contact layers **25** and **27** are patterned to expose the first insulating layer **23** by photolithography.

Referring to FIG. **1E**, conductive metal such as aluminum is laminated on the insulating and ohmic contact layers **23** and **27**. The conductive metal is patterned by photolithography so as to form source electrode **29** and a drain electrode **31**. A portion of the ohmic contact layer **27** exposed between the source and drain electrodes **29** and **31** is etched by using the source and drain electrodes **29** and **31** as masks.

Referring to FIG. **1F**, silicon oxide or silicon nitride is deposited on the entire surface of the structure to form a second insulating layer **33**. The second insulating layer **33** is etched to expose a designated portion of the drain electrode **31**, thus forming a contact hole **35**. By depositing transparent and conductive material on the second insulating layer **33** and patterning it via photolithography, a pixel electrode **37** is formed so as to be electrically connected to the drain electrode **31** through the contact hole **35**.

According to the method of fabricating a thin-film transistor as described above and shown in FIGS. **1A–1F**, respective first and second metal layers are formed through

photolithography using different masks so as to form the gate with a double-layered metal structure, resulting in double step differences between the gate and substrate.

As a result of the double step difference between the gate **21** and the substrate **11** shown in FIG. **1**C, a hillock often occurs on both side portions of the first metal layer **13** which have no portion of the second metal layer **17** deposited thereon when the first metal layer **13** is wider than the second metal layer **17** as in FIG. **1**C. Another problem with this related art method is that the process for forming a gate is complex and requires two photoresists **15**, **19** and two steps of deposition and photolithography. As a result, the contact resistance between the first and second metal layers may be increased.

Another related art method of forming a double metal layer gate structure is described in "Low Cost, High Quality TFT-LCD Process", SOCIETY FOR INFORMATION DISPLAY EURO DISPLAY 96, Proceedings of the 16th International Display Research Conference, Birmingham, England, Oct. 1, 1996, pages 591–594. One page 592 of this publication, a method of forming a double metal gate structure includes the process of depositing two metal layers first and then patterning the two metal layer to thereby eliminate an additional photoresist step. However, with this method, process difficulties during the one step photoresist process for forming the double metal layer gate resulted in the top layer being wider than the bottom layer causing an overhang condition in which the top layer overhangs the bottom layer. This difficulty may result in poor step coverage and disconnection. This problem was solved by using a three-step etching process in which the photoresist had to be baked before each of the three etching steps to avoid lift-off or removal of the photoresist during etching. This three-step etching process and required baking of the photoresist significantly increases the complexity and steps of the gate forming method.

SUMMARY OF THE INVENTION

To overcome the problems discussed above, the preferred embodiments of the present invention provide a thin-film transistor which prevents a hillock and deterioration of step coverage of a later formed gate oxide layer on a double metal layer gate.

The preferred embodiments of the present invention also provide a method of fabricating a thin-film transistor that simplifies the process for forming a double metal layer gate.

The preferred embodiments of the present invention further provide a method of fabricating a thin-film transistor that reduces the contact resistance between the first and second metal layers constituting a gate.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof, as well as, the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the preferred embodiments of the present invention, as embodied and broadly described, a thin-film transistor preferably comprises a substrate, and a gate including a double-layered structure of first and second metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μm, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a desired width on the second metal layer; patterning the second metal layer via an isotropic etching using the photoresist as a mask; patterning the first metal layer via an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have a desired width, thus forming a gate having a laminated structure of the first and second layers; and removing the photoresist.

These and other elements, features, and advantages of the preferred embodiments of the present invention will be apparent from the following detailed description of the preferred embodiments of the present invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate preferred embodiments of the invention and together with the description serve to explain the principles of the invention, in which:

FIGS. **1**A through **1**F are diagrams illustrating a process for fabricating a thin-film transistor according to a method of the related art;

FIG. **2** is a top view of a thin-film transistor according to a preferred embodiment of the present invention;

FIG. **3** is a cross-sectional view taken along line III—III of FIG. **2**; and

FIGS. **4**A through **4**F are diagrams illustrating a process for fabricating a thin-film transistor of preferred embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIG. **2** is a top view of a thin-film transistor according to a preferred embodiment of the present invention. FIG. **3** is a cross-sectional view taken along line III—III of FIG. **2**.

The thin-film transistor comprises a gate **49** having a double-layered structure of a first metal layer **43**, a second metal layer **45** disposed on a substrate **41**, a first insulating layer **51**, a second insulating layers **61**, a semiconductor layer **53**, an ohmic contact layer **55**, a source electrode **57**, a drain electrode **59**, and a pixel electrode **65**.

The gate **49** has a double-layered structure including the first and second metal layers **43** and **45** disposed on the substrate **41**. The first metal layer **43** is preferably formed from a conductive metal such as Al, Cu, or Au deposited to have a certain width w1. The second metal layer **45** is preferably formed from a refractory metal such as Mo, Ta, or Co deposited to have a certain width w2.

The present inventors have discovered that a relationship between the width of the first metal layer and the width of the second metal layer of a double metal layer gate electrode is critical to preventing deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate. More specifically, the present inventors determined that a structure wherein the first metal layer **43** is wider than the second metal layer **45** by about 1 to 4 μm, for example, 1 μm<w1−w2<4 μm, provides maximum prevention of deterioration of step coverage of a later formed gate oxide layer

in such a structure having a double step difference between the substrate and the gate.

To achieve the best results, the second metal layer **45** is preferably positioned substantially in the middle of the first metal layer **45**, so that both side portions of the first metal layer **43** which have no portion of the second metal layer **45** disposed thereon have substantially the same width as each other. The width of each of the side portions is preferably larger than about 0.5 μm but less than about 2 μm.

The first insulating layer **51** is preferably formed by depositing single layer of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the substrate including the gate **49**.

The semiconductor and ohmic contact layers **53** and **55** are formed on the portion of the first insulating layer **51** corresponding to the gate **49** by sequentially depositing undoped amorphous silicon and heavily doped amorphous silicon and patterning the two silicon layers. The semiconductor layer **53** is used as the active region of an element, thus forming a channel by means of a voltage applied to the gate **49**. The ohmic contact layer **55** provides an ohmic contact between the semiconductor layer **53** and the source and drain electrodes **57** and **59**. The ohmic contact layer **55** is not formed in the portion that becomes the channel of the semiconductor layer **53**.

The source and drain electrodes **57** and **59** are in contact with the ohmic contact layer **55**, and each electrode **57**, **59** extends to a designated portion on the first insulating layer **51**.

The second insulating layer **61** is formed by depositing insulating material such as silicon oxide SiO_2 silicon nitride Si_3N_4 to cover the source and drain electrodes **57** and **59** and the first insulating layer **51**. The second insulating layer **61** on the drain electrode **59** is removed to form a contact hole **63**. The pixel electrode **65** is formed from transparent and conductive material such as ITO (Indium Tin Oxide) or Tin oxide SnO_2, so that it is connected to the drain electrode **59** through the contact hole **63**.

In the first and second metal layers **43** and **45** constituting the gate **49**, each side portion of the first metal layer **43** having no portion of the second metal layer **45** thereon has a width that is preferably larger than about 0.5 μm and less than about 2 μm. Because the first metal layer **43** is wider than the second metal layer **45** by about 1.0 μm to 4.0 μm, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate **49** and substrate **41**. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer **51** which deterioration occurs in prior art devices. The hillock in the first metal layer **43** is also avoidable because the width difference between the first and second metal layers **43** and **45** is between about 1 μm to 4 μm.

FIGS. **4**A through **4**F are diagrams illustrating the process for fabricating the thin-film transistor of the preferred embodiments of the present invention.

Referring to FIG. **4**A, metal such as Al, Cu, or Au is deposited on a substrate so as to form a first metal layer **43**. A second metal layer **45** is formed from Mo, Ta, or Co and deposited on the first metal layer **43** without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers **43** and **45** are sequentially deposited so as to preferably have a thickness as large as about 500–4000 Angstroms and 500–2000 Angstroms, respectively, by means of sputtering or chemical vapor deposition (hereinafter, referred to as CVD) without breaking a vacuum state. As a result, the contact resistance between the first and second metal layers **43** and **45** is reduced.

According to the preferred embodiments of the present invention, a single photoresist step is used to pattern both the first metal layer **43** and the second metal layer **45** simultaneously. In the single photoresist step, a photoresist **47** is deposited on the second metal layer **45** and then the photoresist **47** is patterned through exposure and development to have the width w1 on a designated portion of the second metal layer **45**.

Referring to FIG. **4**B, the second metal layer **45** is patterned with an etching solution preferably prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3, by means of a wet etching using the photoresist **47** as a mask. Because the portion of the second metal layer **45** covered with the photoresist **47**, as well as, exposed side portions of the second metal layer **45** are isotropically etched, the second metal layer **45** is preferably patterned to have the width w2 which is narrower than the width w1 of the photoresist **47** which is the same as the width w1 of the first metal layer **43**, that is, about 1 μm<w1−w2<4 μm. Each side portion of the second metal layer **45** preferably has a width larger than about 0.5 μm and less than about 2 μm. That is, the two side portions of the second metal layer **45** covered with the photoresist **47** are preferably etched to have substantially the same width as each other. The lateral surfaces of the second metal layer **45** are preferably etched to have a substantially rectangular or inclined shape.

Referring to FIG. **4**C, the first metal layer **43** is patterned via dry etching having anisotropic etching characteristic such as reactive ion etching (hereinafter, referred to as RIE) by using the photoresist **47** as a mask. When etching the first metal layer **43** other than the portion of the layer **43** covered with the photoresist **47**, the first metal layer **43** preferably has the same width w1 of the photoresist **47**. Thus, patterning of the first and second metal layers **43**, **45**, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the relation between the first and second metal layers **43** and **45** also may be represented by about 1 μm<w1−w2<4 μm.

The first and second metal layers **43** and **45** resulting form the single photoresist step process described above form a gate **49** having a double-layered metal structure. The gate **49** has the second metal layer **45** positioned substantially in the middle of the first metal layer **43** so that the each side portion of the first metal layer **43** having no second metal layer **45** thereon is wider than about 0.5 μm but narrower than about 2 μm. The photoresist **47** remaining on the second metal layer **45** is removed after the two etching steps are completed.

Referring to FIG. **4**D, a first insulating layer **51** is formed by depositing a single layer or double layers of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the gate **49** and substrate **41** by CVD. Because each side portion of the first metal layer **43** having no second metal layer **45** thereon is wider than 0.5 μm, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer **51** from being deteriorated as in prior art devices. The hillock in the first metal layer **43** is also avoidable because a width of a portion of the first metal layer **43** which is exposed is less than about 2 μm.

Amorphous silicon which is undoped and heavily doped amorphous silicon are sequentially deposited on the first

insulating layer **41** by CVD, thus forming semiconductor and ohmic contact layers **53** and **55**. The ohmic contact and semiconductor layers **55** and **53** are patterned by means of photolithography to expose the first insulating layer **51**.

Referring to FIG. **4**E, conductive metal such as Al or Cr is laminated on the insulating and ohmic contact layers **51** and **55** and patterned by photolithography to form source and drain electrodes **57** and **59**. The ohmic contact layer **55** exposed between the source and drain electrodes **57** and **59** is etched by using the source drain electrodes **57** and **59** as masks.

Referring to FIG. **4**F, a second insulating layer **61** is formed by depositing insulating material such as silicon oxide or silicon nitride by CVD on the entire surface of the above structure. The second insulating layer is removed by photolithography to expose a designated portion of the drain electrode **59** and thus form a contact hole **63**. Once transparent and conductive material such as ITO (Indium Tin Oxide) or Tin oxide SnO_2 is deposited on the second insulating layer **61** via sputtering and patterned by photolithography, a pixel electrode **65** is formed so that it is electrically connected to the drain electrode **59** through the contact hole **63**.

In another preferred embodiment of the present invention, the first and second metal layers **43** and **45** are first etched by means of a dry etching having anisotropic etching characteristic such as RIE by using the photoresist **47** as a mask. The gate **49** is formed by etching the second metal layer **45** under the photoresist **47** with an etching solution prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3.

In still another preferred embodiment of the present invention, the gate **49** is formed through a single etching step process for etching the first and second metal layers **43** and **45** simultaneously and via a single etching step, where the second metal layer **45** is etched more quickly than the first metal layer **43** with an etching solution prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3. Because of the etching material and metals used for the first and second metal layers of the gate, only a single etching step is required. Despite the fact that a single etching step is used, it is still possible to obtain the relationship between the widths w1 and w2 of the first and second metal layers described above. In this process, the first and second metal layers forming the gate **49** are formed and patterned with a single photo resist step as described above and a single etching step.

As described above, in the preferred embodiments of the present invention, the first and second metal layers are sequentially deposited on the substrate without performing a masking step between the step of depositing the first metal layer and the second metal layer, followed by forming a photoresist that covers a designated portion of the second metal layer. In one preferred embodiment, the second metal layer is wet etched by using the photoresist as a mask but the first metal layer is dry etched. As a result, the double-metal gate is formed. In another preferred embodiment, a single etching step is used to form the double-metal gate wherein both the first metal layer and the second metal layer are wet etched, but the difference in etching rates of the first and second metal layers produces different etching affects which result in the desired double-step structure.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a photoresist having a predetermined width on the second metal layer;

anisotropically etching the first and second metal layers so such that the first metal layer and the second metal layer have the same width of the photoresist by using the photoresist as a mask,

isotropically etching the second metal layer such that the second metal layer is narrower than the first metal layer by about 1 μm to about 4 μm by using the photoresist as a mask, thus forming a gate having a double-layered structure including the first and second metal layers; and removing the photoresist.

2. The method of making a thin-film transistor as claimed in claim **1**, further comprising the steps of:

forming a first insulating layer on the substrate including the gate;

forming a semiconductor layer and an ohmic contact layer on a portion of the first insulating layer at a location corresponding to the gate;

forming a source electrode and drain electrode extending onto the first insulating layer on two sides of the ohmic contact layer, and removing a portion of the ohmic contact layer exposed between the source and drain electrodes; and

forming a second insulating layer covering the semiconductor layer, the source electrode, the drain electrode and the first insulating layer.

3. The method of making a thin-film transistor as claimed in claim **1**, wherein the first metal layer includes Al, Cu, or Au.

4. The method of making a thin-film transistor as claimed in claim **1**, wherein the second metal layer includes Mo, Ta, or Co.

5. The method of making a thin-film transistor as claimed in claim **1**, wherein the first and second metal layers are removed via a dry etching method.

6. The method of making a thin-film transistor as claimed in claim **1**, wherein the second metal layer is etched with an etching solution prepared with a mixture of phosphoric acid, acetic acid and nitric acid.

7. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer;

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.

8. The method of claim **7**, wherein the first and second metal layers are patterned so that the first metal layer has a first and a second side portion being exposed from the second metal layer, each side portion being at least about 0.5 μm in width.

9. The method of claim **8**, wherein each side portion of the first metal layer is exposed so that each side portion is less than about 2 μm in width.

10. The method of claim **7**, wherein the patterning step is such that the second metal layer is etched faster than the first etching layer.

11. The method of claim **10**, wherein the second metal layer is wet etched, and the first metal layer is dry etched.

12. The method of claim **10**, wherein both the first and second metal layers are wet etched.

13. The method of claim **7**, wherein the patterning step comprises:

isotropically etching the second metal layer; and

anisotropically etching the first metal layer.

14. The method of claim **7**, wherein no masking step is required between the formation of the first and second metal layers.

15. The method of claim **7**, wherein the patterning step does not require processing of a photoresist before etching.

16. A method of waking a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm; and

removing the photoresist.

17. The method of making a thin film transistor as claimed in claim **16**, further comprising the steps of:

forming a first insulating layer on the substrate including the gate;

forming a semiconductor layer and an ohmic contact layer on a portion of the first insulating layer at a location corresponding to the gate;

forming a source electrode and a drain electrode extending onto the first insulating layer on two sides of the ohmic contact layer, and removing a portion of the ohmic contact layer exposed between the source and the drain electrodes; and

forming a second insulating layer covering the semiconductor layer, the source electrode, the drain electrode and the first insulating layer.

18. The method of making a thin film transistor as claimed in claim **16**, wherein the first and second metal layers are sequentially deposited via sputtering or a chemical vapor deposition method without breaking a vacuum state.

19. The method of making a thin film transistor as claimed in claim **16**, wherein the first metal layer has thickness of about 500 Å to about 4000 Å.

20. The method of making a thin film transistor as claimed in claim **16**, wherein the second metal layer includes Mo, Ta or Co.

21. The method of making a thin film transistor as claimed in claim **16**, wherein the first metal layer has a thickness of about 500 Å to about 2000 Å.

22. The method of making a thin film transistor as claimed in claim **16**, wherein two side portions of the first metal layer having no second metal layer deposited thereon have substantially the same width as each other.

* * * * *

Exhibit C

US005905274A

United States Patent [19]

Ahn et al.

[11] Patent Number: 5,905,274

[45] Date of Patent: May 18, 1999

[54] **THIN-FILM TRANSISTOR AND METHOD OF MAKING SAME**

[75] Inventors: **Byung-Chul Ahn**, Kumi-shi; **Hyun-Sik Seo**, Anyang-shi, both of Rep. of Korea

[73] Assignee: **L.G. Electronics, Inc.**, Youngdungpo-ku, Japan

[21] Appl. No.: **08/918,119**

[22] Filed: **Aug. 27, 1997**

[30] **Foreign Application Priority Data**

Mar. 4, 1997 [KR] Rep. of Korea 97-7010

[51] **Int. Cl.**[6] **H01L 29/04**; H01L 31/036; H01L 31/0376

[52] **U.S. Cl.** **257/59**; 257/61; 257/72; 257/350

[58] **Field of Search** 257/57, 58, 59, 257/60, 61, 66, 72, 350

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,036,370	7/1991	Miyago et al. .	
5,132,745	7/1992	Kwasnick et al. .	
5,156,986	10/1992	Wei et al.	437/40
5,428,250	6/1995	Ikeda et al.	257/761

FOREIGN PATENT DOCUMENTS

0602315	7/1993	European Pat. Off. .
03114028	5/1991	Japan .
6-37311	2/1994	Japan .
2254187	9/1992	United Kingdom .

OTHER PUBLICATIONS

"Low Cost, High Display Quality TFT–LCD Process", Society for Information Display, EuroDisplay 96, Proceedings of the 16th International Display Research Conference, Oct. 1, 1996, 591–594.

"Hilllock–Free A1–Gate Materials Using Stress–Absorbing Buffer Layer for Large Area AMLCDs" Society for Information Display 96 Digest, pp. 341–344, 1996.

Primary Examiner—Ngân V. Ngô

Attorney, Agent, or Firm—Graham & James LLP

[57] **ABSTRACT**

A thin-film transistor includes a substrate and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μm. A method of making such a thin film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

6 Claims, 6 Drawing Sheets

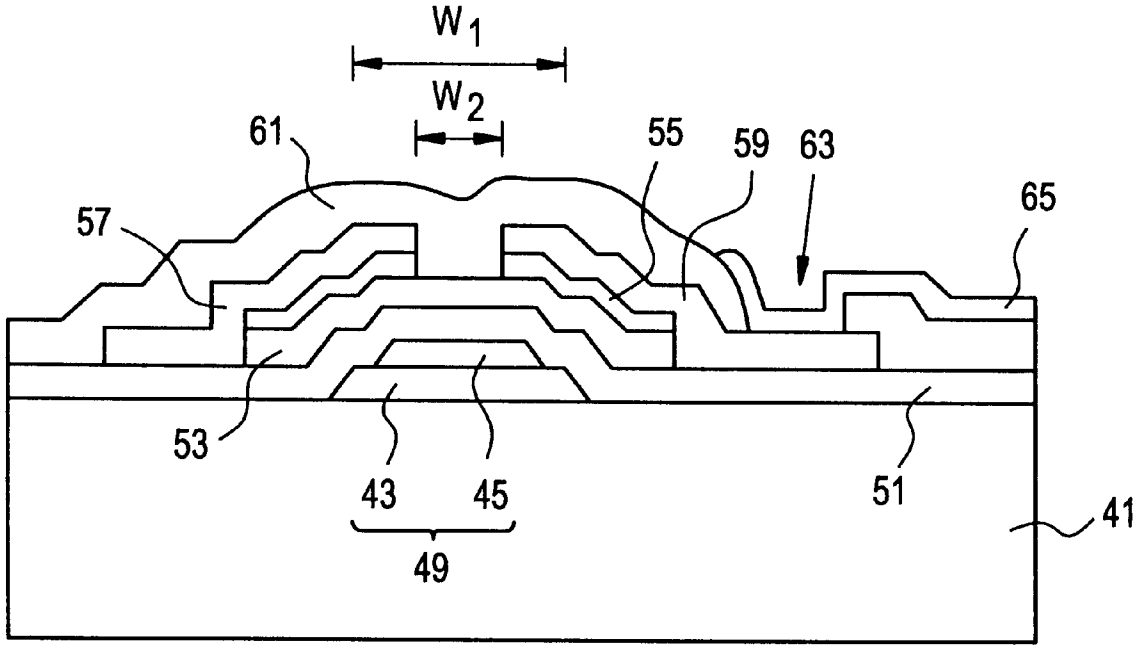


FIG. 1A

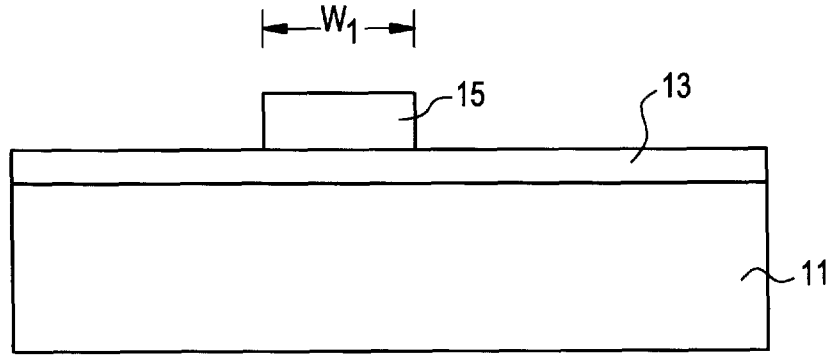


FIG. 1B

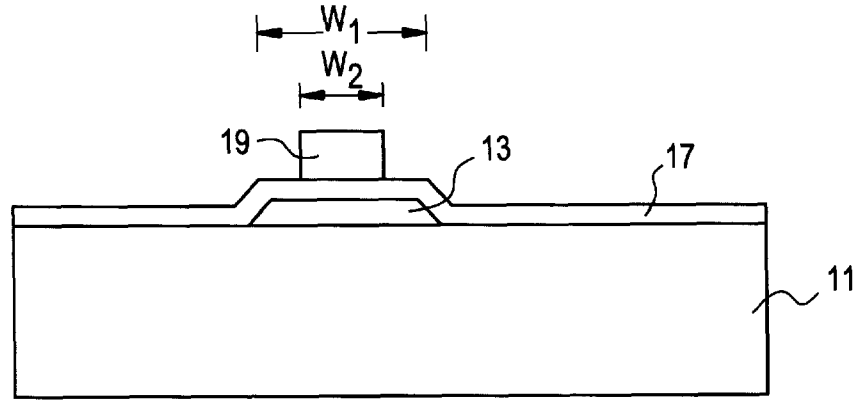


FIG. 1C

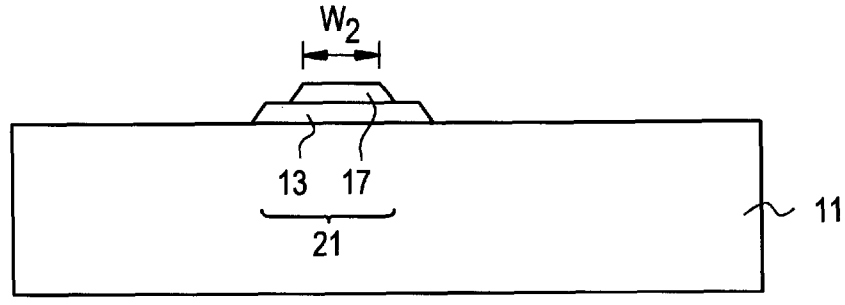


FIG. 1D

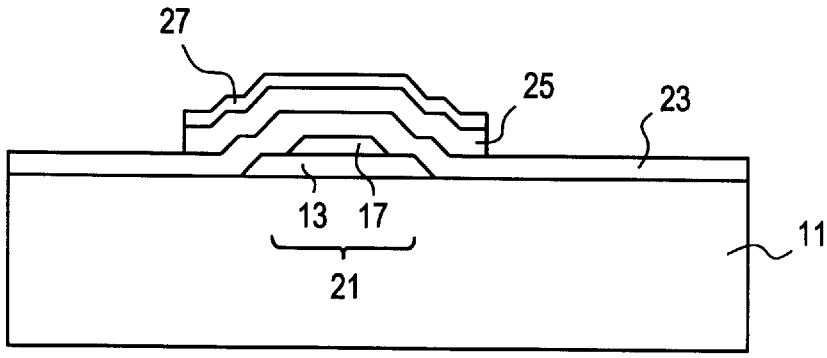


FIG. 1E

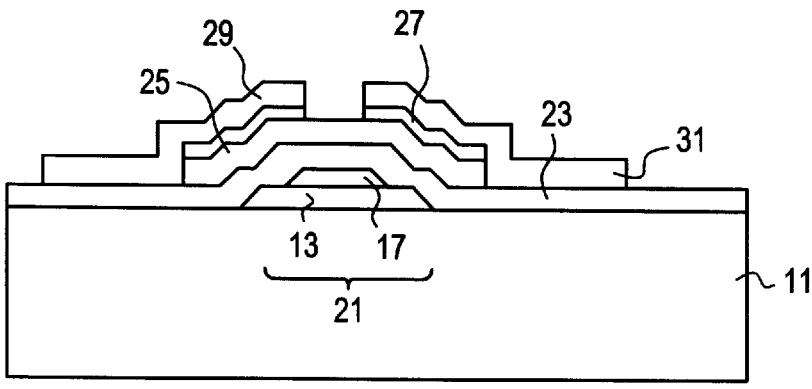


FIG. 1F

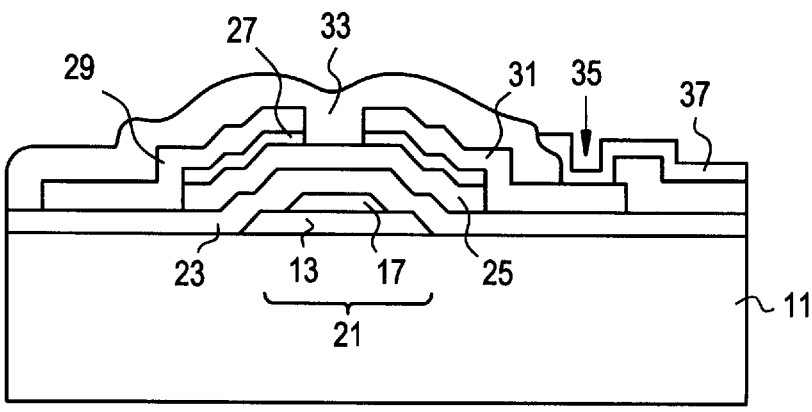


FIG. 2

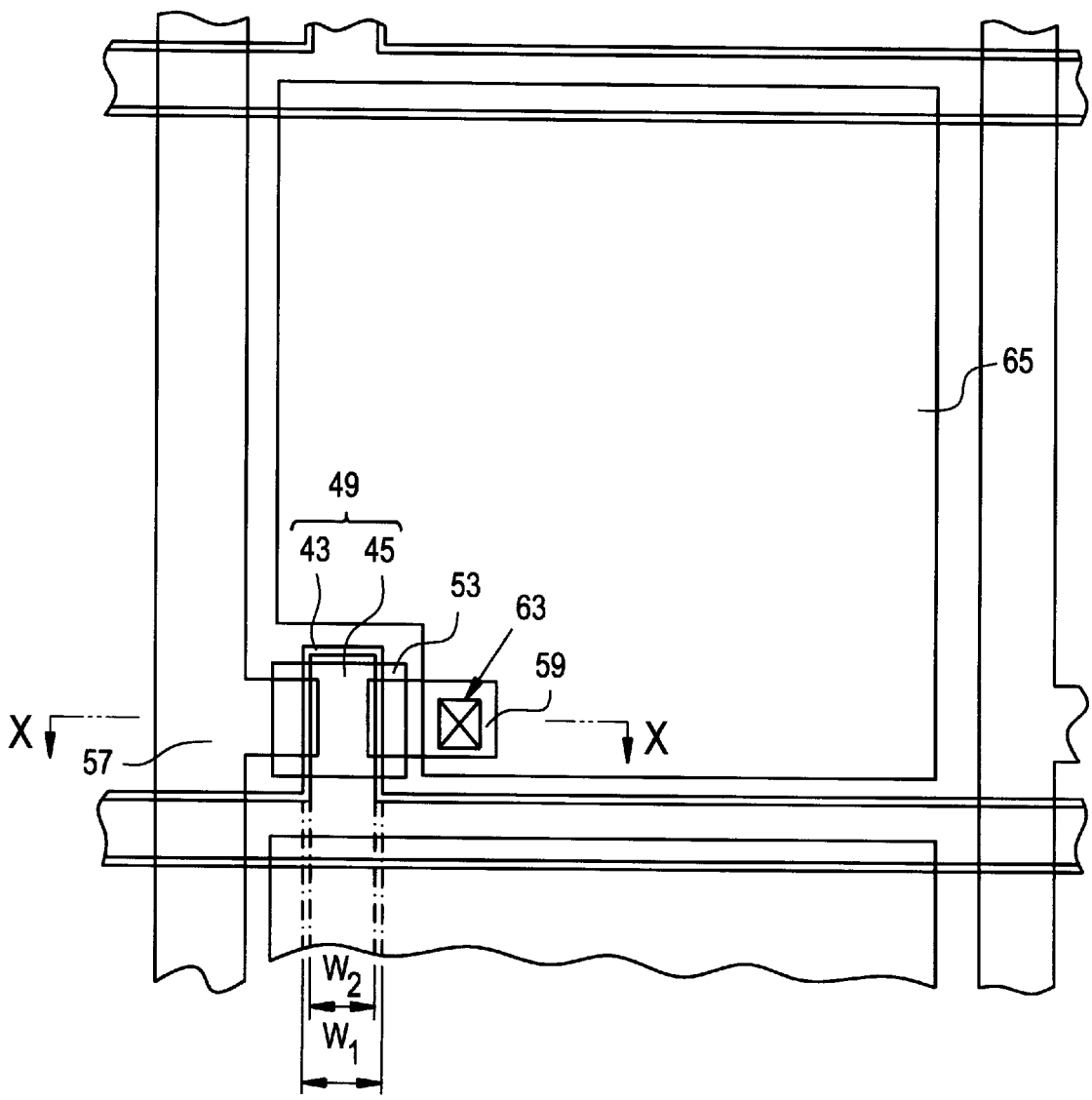


FIG. 3

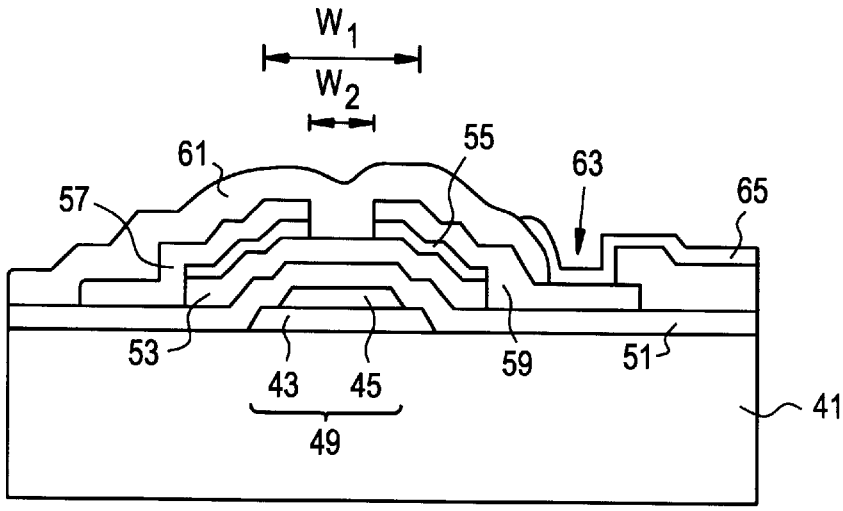


FIG. 4A

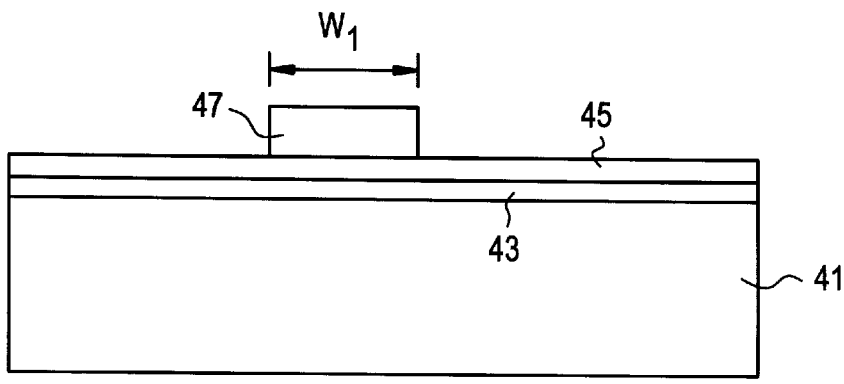


FIG. 4B

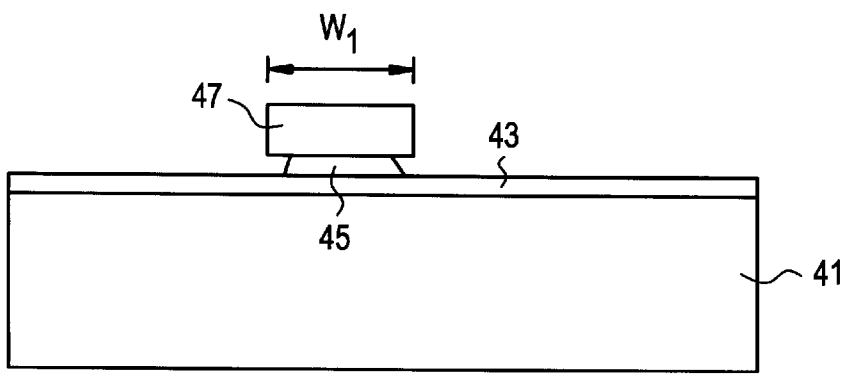


FIG. 4C

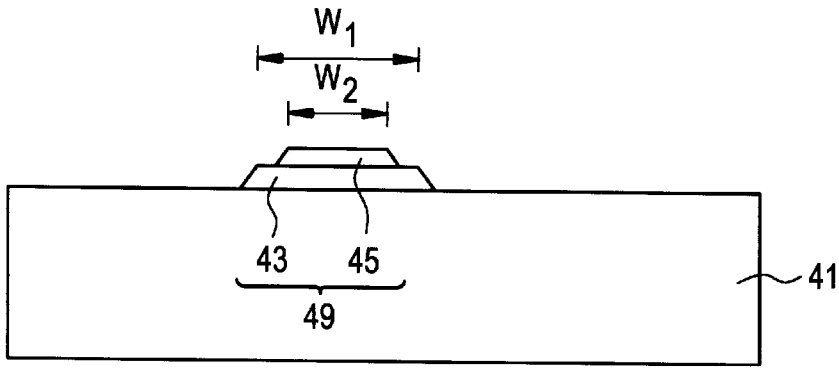


FIG. 4D

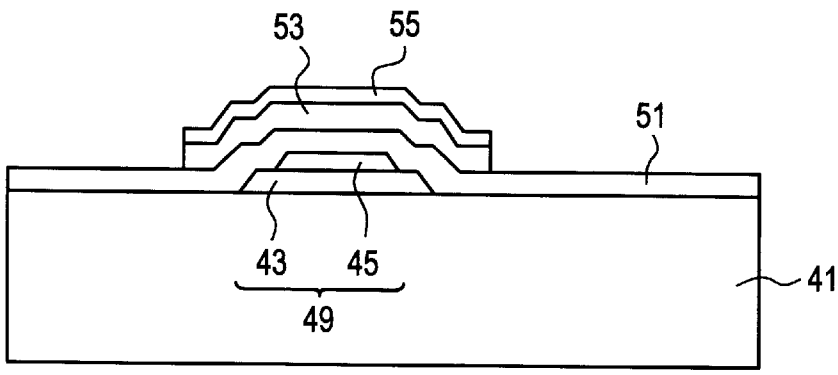


FIG. 4E

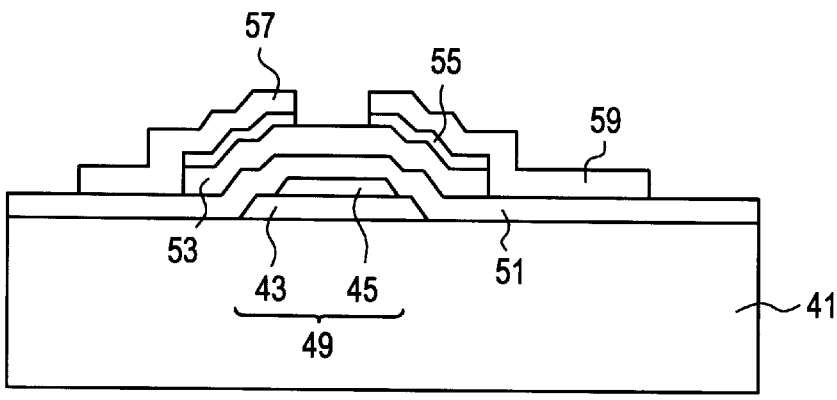
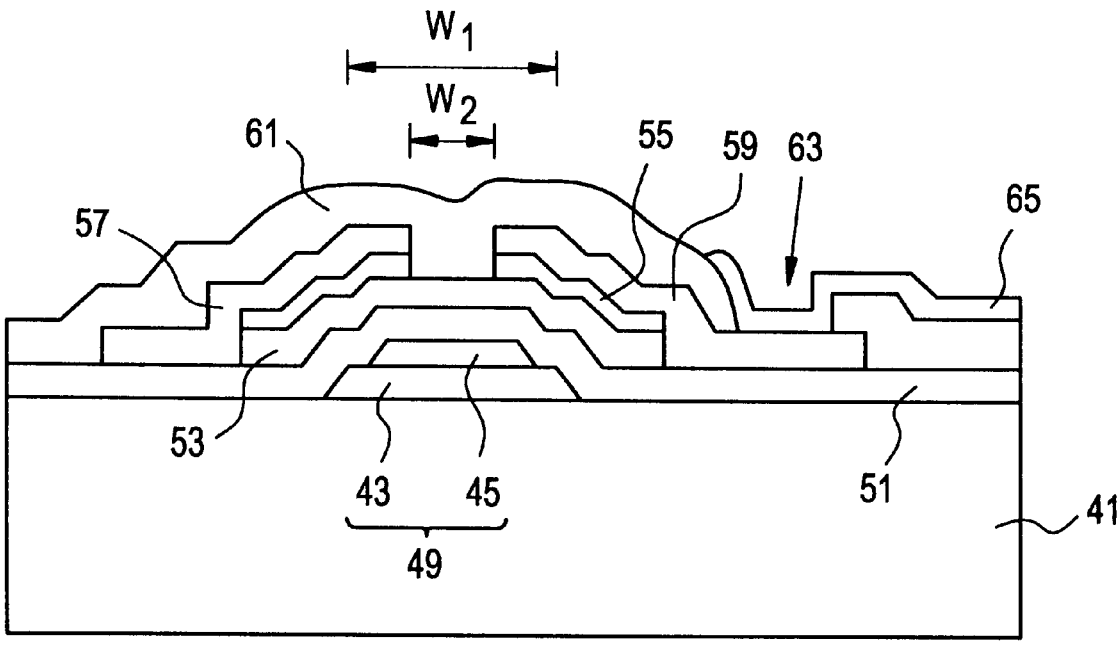


FIG. 4F



THIN-FILM TRANSISTOR AND METHOD OF MAKING SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a thin-film transistor of a liquid crystal display and, more particularly, to a thin-film transistor having a gate including a double-layered metal structure and a method of making such a double-layered metal gate.

2. Discussion of Related Art

An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electrodes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

The gate of the thin-film transistor is made of aluminum to reduce its wiring resistance, but an aluminum gate may cause defects such as hillock.

A double-layered metal gate, i.e., molybdenum-coated aluminum gate is considered as a substitute for the aluminum gate to overcome the problem of the hillock.

To fabricate a double-layered gate, metals such as aluminum and molybdenum are sequentially deposited, followed by a patterning process carried out via photolithography to form resulting metal films which have the same width. Although the double-layered gate is desirable to overcome the problem of hillock, the resulting deposited metal films forming the double-layered gate are so thick that a severe single step is created by a thickness difference between the metal films and a substrate, thereby causing a single step difference between the substrate and the double-layered gate which deteriorates the step coverage of a later formed gate oxide layer. The source and drain regions formed on the gate oxide layer may have disconnections between areas of the source and drain regions which are overlapped and non-overlapped with the gate, or electrically exhibit short circuits as a result of contact with the gate.

According to another method of forming the gate, each of the metal layers of Al and Mo form a double step difference with the substrate so as to improve the step coverage of the gate oxide layer.

FIGS. **1**A through **1**F are diagrams illustrating the process for fabricating a thin-film transistor of a method which is related to the invention described and claimed in the present application. The method shown in FIGS. **1**A–**1**F is not believed to be published prior art but is merely a recently discovered method related to the invention described and claimed in the present application.

Referring to FIG. **1**A, aluminum is deposited on a substrate **11** to form a first metal layer **13**. A first photoresist **15** is deposited on the first metal layer **13**. The first photoresist **15** is exposed and developed so as to have a certain width w**1** extending along the first metal layer **13**.

Referring to FIG. **1**B, the first metal layer **13** is patterned via wet etching using the first photoresist **15** as a mask so that the first metal layer **13** has a certain width w**1**. After the first photoresist **15** is removed, a second metal layer **17** is formed by depositing Mo, Ta, or Co on the substrate **11** so as to cover the first metal layer **13**. A second photoresist **19** is then deposited on the second metal layer **17**. The second photoresist **19** is exposed and developed so as to have a certain width w**2** extending along the second metal layer **17** and located above the first metal layer **13**.

Referring to FIG. **1**C, the second metal layer **17** is patterned via a wet etching process using the second photoresist **19** as a mask such that the second metal layer **17** has a certain width w**2** which is narrower than the width w**1** of the first metal layer **13**. After formation of the gate **21**, the second photoresist **19** is removed.

Thus, the patterned first and second metal layers **13** and **17** form a gate **21** having a double-layered metal structure that provides a double step difference between the double-layered metal gate structure **21** and the substrate **11**. The formation of the gate **21** as described above and shown in FIGS. **1**–**3** requires the use of two photoresists **15**, **19** and two photoresist steps.

In the gate **21** shown in FIG. **3**, the second metal layer **17** is preferably centrally located on the first metal layer **13**. Although there is no specific information available regarding a relationship of w**1** to w**2** of this related method, based on their understanding of this related method resulting in the structure shown in FIG. **3**, the inventors of the invention described and claimed in the present application assume that the width difference w**1**–w**2** between the first and second metal layers **13** and **17** is larger than or equal to 4 μm, that is, w**1**–w**2**$\geqq$4 μm.

Referring to FIG. **1**D, a first insulating layer **23** is formed by depositing silicon oxide SiO_2 or silicon nitride Si_3N_4 as a single-layered or double-layered structure on the gate **21** and substrate **11**. Semiconductor and ohmic contact layers **25** and **27** are formed by sequentially depositing undoped polycrystalline silicon and heavily doped silicon on the first insulating layer **23**. The semiconductor and ohmic contact layers **25** and **27** are patterned to expose the first insulating layer **23** by photolithography.

Referring to FIG. **1**E, conductive metal such as aluminum is laminated on the insulating and ohmic contact layers **23** and **27**. The conductive metal is patterned by photolithography so as to form a source electrode **29** and a drain electrode **31**. A portion of the ohmic contact layer **27** exposed between the source and drain electrodes **29** and **31** is etched by using the source and drain electrodes **29** and **31** as masks.

Referring to FIG. **1**F, silicon oxide or silicon nitride is deposited on the entire surface of the structure to form a second insulating layer **33**. The second insulating layer **33** is etched to expose a designated portion of the drain electrode **31**, thus forming a contact hole **35**. By depositing transparent and conductive material on the second insulating layer **33** and patterning it via photolithography, a pixel electrode **37** is formed so as to be electrically connected to the drain electrode **31** through the contact hole **35**.

According to the method of fabricating a thin-film transistor as described above and shown in FIGS. **1**A–**1**F, respective first and second metal layers are formed through photolithography using different masks so as to form the gate with a double-layered metal structure, resulting in double step differences between the gate and substrate.

As a result of the double step difference between the gate **21** and the substrate **11** shown in FIG. **1**C, a hillock often occurs on both side portions of the first metal layer **13** which have no portion of the second metal layer **17** deposited thereon when the first metal layer **13** is wider than the second metal layer **17** as in FIG. **1**C. Another problem with this related method is that the process for forming a gate is complex and requires two photoresists **15**, **19** and two steps of deposition and photolithography. As a result, the contact resistance between the first and second metal layers may be increased.

Another method of forming a double metal layer gate structure is described in "Low Cost, High Quality TFT-LCD

Process", SOCIETY FOR INFORMATION DISPLAY EURO DISPLAY 96, Proceedings of the 16th International Display Research Conference, Birmingham, England, Oct. 1, 1996, pages 591–594. On page 592 of this publication, a method of forming a double metal gate structure includes the process of depositing two metal layers first and then patterning the two metal layers to thereby eliminate an additional photoresist step. However, with this method, process difficulties during the one step photoresist process for forming the double metal layer gate resulted in the top layer being wider than the bottom layer causing an overhang condition in which the top layer overhangs the bottom layer. This difficulty may result in poor step coverage and disconnection. This problem was solved by using a three-step etching process in which the photoresist had to be baked before each of the three etching steps to avoid lift-off or removal of the photoresist during etching. This three-step etching process and required baking of the photoresist significantly increases the complexity and steps of the gate forming method.

SUMMARY OF THE INVENTION

To overcome the problems discussed above, the preferred embodiments of the present invention provide a thin-film transistor which prevents a hillock and deterioration of step coverage of a later formed gate oxide layer on a double metal layer gate.

The preferred embodiments of the present invention also provide a method of fabricating a thin-film transistor that simplifies the process for forming a double metal layer gate.

The preferred embodiments of the present invention further provide a method of fabricating a thin-film transistor that reduces the contact resistance between the first and second metal layers constituting a gate.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof, as well as, the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the preferred embodiments of the present invention, as embodied and broadly described, a thin-film transistor preferably comprises a substrate, and a gate including a double-layered structure of first and second metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μm, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a desired width on the second metal layer; patterning the second metal layer via an isotropic etching using the photoresist as a mask; patterning the first metal layer via an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have a desired width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

These and other elements, features, and advantages of the preferred embodiments of the present invention will be apparent from the following detailed description of the preferred embodiments of the present invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate preferred embodiments of the invention and together with the description serve to explain the principles of the invention, in which:

FIGS. **1**A through **1**F are diagrams illustrating a process for fabricating a thin-film transistor according to a method which is related to the preferred embodiments of the present invention;

FIG. **2** is a top view of a thin-film transistor according to a preferred embodiment of the present invention;

FIG. **3** is a cross-sectional view taken along line X—X of FIG. **2**; and

FIGS. **4**A through **4**F are diagrams illustrating a process for fabricating a thin-film transistor of preferred embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIG. **2** is a top view of a thin-film transistor according to a preferred embodiment of the present invention. FIG. **3** is a cross-sectional view taken along line x—x of FIG. **2**.

The thin-film transistor comprises a gate **49** having a double-layered structure of a first metal layer **43**, a second metal layer **45** disposed on a substrate **41**, a first insulating layer **51**, a second insulating layer **61**, a semiconductor layer **53**, an ohmic contact layer **55**, a source electrode **57**, a drain electrode **59**, and a pixel electrode **65**.

The gate **49** has a double-layered structure including the first and second metal layers **43** and **45** disposed on the substrate **41**. The first metal layer **43** is preferably formed from a conductive metal such as Al, Cu, or Au deposited to have a certain width w**1**. The second metal layer **45** is preferably formed from a refractory metal such as Mo, Ta, or Co deposited to have a certain width w**2**.

The present inventors have discovered that a relationship between the width of the first metal layer and the width of the second metal layer of a double metal layer gate electrode is critical to preventing deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate. More specifically, the present inventors determined that a structure wherein the first metal layer **43** is wider than the second metal layer **45** by about 1 to 4 μm, for example, 1 μm<w**1**–w**2**<4 μm, provides maximum prevention of deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate.

To achieve the best results, the second metal layer **45** is preferably positioned substantially in the middle of the first metal layer **45**, so that both side portions of the first metal layer **43** which have no portion of the second metal layer **45** disposed thereon have substantially the same width as each other. The width of each of the side portions is preferably larger than about 0.5 μm but less than about 2 μm.

The first insulating layer **51** is preferably formed by depositing single layer of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the substrate including the gate **49**.

The semiconductor and ohmic contact layers **53** and **55** are formed on the portion of the first insulating layer **51** corresponding to the gate **49** by sequentially depositing undoped amorphous silicon and heavily doped amorphous silicon and patterning the two silicon layers. The semicon-

ductor layer **53** is used as the active region of an element, thus forming a channel by means of a voltage applied to the gate **49**. The ohmic contact layer **55** provides an ohmic contact between the semiconductor layer **53** and the source and drain electrodes **57** and **59**. The ohmic contact layer **55** is not formed in the portion that becomes the channel of the semiconductor layer **53**.

The source and drain electrodes **57** and **59** are in contact with the ohmic contact layer **55**, and each electrode **57**, **59** extends to a designated portion on the first insulating layer **51**.

The second insulating layer **61** is formed by depositing insulating material such as silicon oxide SiO_2 silicon nitride Si_3N_4 to cover the source and drain electrodes **57** and **59** and the first insulating layer **51**. The second insulating layer **61** on the drain electrode **59** is removed to form a contact hole **63**. The pixel electrode **65** is formed from transparent and conductive material such as ITO (Indium Tin Oxide) or Tin oxide SnO_2, so that it is connected to the drain electrode **59** through the contact hole **63**.

In the first and second metal layers **43** and **45** constituting the gate **49**, each side portion of the first metal layer **43** having no portion of the second metal layer **45** thereon has a width that is preferably larger than about 0.5 μm and less than about 2 μm. Because the first metal layer **43** is wider than the second metal layer **45** by about 1.0 μm to 4.0 μm, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate **49** and substrate **41**. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer **51** which deterioration occurs in prior art devices. The hillock in the first metal layer **43** is also avoidable because the width difference between the first and second metal layers **43** and **45** is between about 1 μm to 4 μm.

FIGS. **4**A through **4**F are diagrams illustrating the process for fabricating the thin-film transistor of the preferred embodiments of the present invention.

Referring to FIG. **4**A, metal such as Al, Cu, or Au is deposited on a substrate so as to form a first metal layer **43**. A second metal layer **45** is formed from Mo, Ta, or Co and deposited on the first metal layer **43** without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers **43** and **45** are sequentially deposited so as to preferably have a thickness as large as about 500–4000A and 500–2000A, respectively, by means of sputtering or chemical vapor deposition (hereinafter, referred to as CVD) without breaking a vacuum state. As a result, the contact resistance between the first and second metal layers **43** and **45** is reduced.

According to the preferred embodiments of the present invention, a single photoresist step is used to pattern both the first metal layer **43** and the second metal layer **45** simultaneously. In the single photoresist step, a photoresist **47** is deposited on the second metal layer **45** and then the photoresist **47** is patterned through exposure and development to have the width w**1** on a designated portion of the second metal layer **45**.

Referring to FIG. **4**B, the second metal layer **45** is patterned with an etching solution preferably prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3, by means of a wet etching using the photoresist **47** as a mask. Because the portion of the second metal layer **45** covered with the photoresist **47**, as well as, exposed side portions of the second metal layer **45** are isotopically etched, the second metal layer **45** is preferably patterned to have the width w**2** which is narrower than the width w**1** of the photoresist **47** which is the same as the width w**1** of the first metal layer **43**, that is, about 1 μm<w**1**–w**2**<4 μm. Each side portion of the second metal layer **45** preferably has a width larger than about 0.5 μm and less than about 2 μm. That is, the two side portions of the second metal layer **45** covered with the photoresist **47** are preferably etched to have substantially the same width as each other. The lateral surfaces of the second metal layer **45** are preferably etched to have a substantially rectangular or inclined shape.

Referring to FIG. **4**C, the first metal layer **43** is patterned via a wet etching having anisotropic etching characteristic such as reactive ion etching (hereinafter, referred to as RIE) by using the photoresist **47** as a mask. When etching the first metal layer **43** other than the portion of the layer **43** covered with the photoresist **47**, the first metal layer **43** preferably has the same width w**1** of the photoresist **47**. Thus, patterning of the first and second metal layers **43**, **45**, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the relation between the first and second metal layers **43** and **45** also may be represented by about 1 μm<w**1**–w**2**<4 μm.

The first and second metal layers **43** and **45** resulting from the single photoresist step process described above form a gate **49** having a double-layered metal structure. The gate **49** has the second metal layer **45** positioned substantially in the middle of the first metal layer **43** so that the each side portion of the first metal layer **43** having no second metal layer **45** thereon is wider than about 0.5 μm but narrower than about 2 μm. The photoresist **47** remaining on the second metal layer **45** is removed after the two etching steps are completed.

Referring to FIG. **4**D, a first insulating layer **51** is formed by depositing a single layer or double layers of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the gate **49** and substrate **41** by CVD. Because each side portion of the first metal layer **43** having no second metal layer **45** thereon is wider than about 0.5 μm, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer **51** from being deteriorated as in prior art devices. The hillock in the first metal layer **43** is also avoidable because a width of a portion of the first metal layer **43** which is exposed is less than about 2 μm.

Amorphous silicon which is undoped and heavily doped amorphous silicon are sequentially deposited on the first insulating layer **41** by CVD, thus forming semiconductor and ohmic contact layers **53** and **55**. The ohmic contact and semiconductor layers **55** and **53** are patterned by means of photolithography to expose the first insulating layer **51**.

Referring to FIG. **4**E, conductive metal such as Al or Cr is laminated on the insulating and ohmic contact layers **51** and **55** and patterned by photolithography to form source and drain electrodes **57** and **59**. The ohmic contact layer **55** exposed between the source and drain electrodes **57** and **59** is etched by using the source drain electrodes **57** and **59** as masks.

Referring to FIG. **4**F, a second insulating layer **61** is formed by depositing insulating material such as silicon oxide or silicon nitride by CVD on the entire surface of the above structure. The second insulating layer is removed by photolithography to expose a designated portion of the drain electrode **59** and thus form a contact hole **63**. Once trans-

parent and conductive material such as ITO (Indium Tin Oxide) or Tin oxide SnO_2 is deposited on the second insulating layer **61** via sputtering and patterned by photolithography, a pixel electrode **65** is formed so that it is electrically connected to the drain electrode **59** through the contact hole **63**.

In another preferred embodiment of the present invention, the first and second metal layers **43** and **45** are first etched by means of a dry etching having anisotropic etching characteristic such as RIE by using the photoresist **47** as a mask. The gate **49** is formed by etching the second metal layer **45** under the photoresist **47** with an etching solution prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3.

In still another preferred embodiment of the present invention, the gate **49** is formed through a single etching step process for etching the first and second metal layers **43** and **45** simultaneously and via a single etching step, where the second metal layer **45** is etched more quickly than the first metal layer **43** with an etching solution prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3. Because of the etching material and metals used for the first and second metal layers of the gate, only a single etching step is required. Despite the fact that a single etching step is used, it is still possible to obtain the relationship between the widths w**1** and w**2** of the first and second metal layers described above. In this process, the first and second metal layers forming the gate **49** are formed and patterned with a single photo resist step as described above and a single etching step.

As described above, in the preferred embodiments of the present invention, the first and second metal layers are sequentially deposited on the substrate without performing a masking step between the step of depositing the first metal layer and the second metal layer, followed by forming a photoresist that covers a designated portion of the second metal layer. In one preferred embodiment, the second metal layer is wet etched by using the photoresist as a mask but the first metal layer is dry etched. As a result, the double-metal gate is formed. In another preferred embodiment, a single etching step is used to form the double-metal gate wherein both the first metal layer and the second metal layer are wet etched, but the different in etching rates of the first and second metal layers produces different etching affects which result in the desired double-step structure.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A thin film transistor comprising:

a substrate; and

a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 μm.

2. The thin-film transistor as claimed in claim **1**, wherein the second metal layer is located in a middle portion of the first metal layer so that two side portions of the first metal layer having no second metal layer disposed thereon have the same width as each other.

3. The thin-film transistor as claimed in claim **1**, wherein the second metal layer includes at least one of Mo, Ta, and Co.

4. A thin film transistor comprising:

a substrate;

a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 μm;

a first insulating layer disposed on the substrate including the gate;

a semiconductor layer disposed on a portion of the first insulating layer at a location corresponding to the gate;

an ohmic contact layer disposed on two sides of the semiconductor layer;

a source electrode and a drain electrode disposed on the ohmic contact layer and extending onto the first insulating layer; and

a second insulating layer covering the semiconductor layer, the source and drain electrodes and the first insulating layer.

5. The thin-film transistor as claimed in claim **4**, wherein the second metal layer is located in a middle portion of the first metal layer so that two side portions of the first metal layer having no second layer thereon have the same width as each other.

6. The thin-film transistor as claimed in claim **4**, wherein the second metal layer includes at least one of Mo, Ta, and Co.

* * * * *